"Some Studies in Performance Enhancement of Permanent Magnet Synchronous Motor Drive in Automotive Application"

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Certificate

This is to certify that the thesis entitled, **"Some Studies in Performance Enhancement of Permanent Magnet Synchronous Motor Drive in Automotive Application"**, submitted by **Rakesh.G.Shriwastava** towards partial fulfillment for the award of Degree of Doctor of Philosophy (Ph.D.) in Electrical Engineering in the faculty of Engineering and Technology of RashtraSant Tukadoji Maharaj Nagpur University, Nagpur is bonafide research work carried out by him under my supervision and guidance. The contents have not been submitted to any other institute for the award of any Degree or Diploma. It is further certified that references made to the works of others have been cited in the text. This certificate is given on the basis of similarity index checked by the candidate which is below 20%.

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Candidate Declaration

I, **Rakesh. G. Shriwastava** (Ph.D. Registration No. Ph.D (Cell) /RRC/E&T/307B/645 w.e.f. 18-02-2011 hereby declare that I have completed the work towards the degree of Doctor of Philosophy (Ph.D.) of RashtraSant Tukadoji Maharaj Nagpur University, Nagpur in Electrical Engineering discipline in the faculty of Engineering and Technology on the topic entitled **"Some Studies in Performance Enhancement of Permanent Magnet Synchronous Motor Drive in Automotive Application"** under the supervision and guidance of **Dr. M. B. Daigavane (Supervisor) & Dr. S. R.Vaishnav (Co-supervisor)**.This thesis embodies the original research work done by me in partial fulfillment of the degree of Doctor of Philosophy of Rashtrasant Tukadoji Maharaj Nagpur University, Nagpur. References made to the work of others have been properly cited in the text. The similarity index is checked using standard tools. It is less than 20%.

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Last but not least, I would like to thank my family members, for their support and co-operation in completing this research work. I would like to share this moment of happiness with them.

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Contents

Abstract

Motivation

The permanent magnet synchronous motor (PMSM) can offer many advantages, including high power-to-weight ratio, high efficiency, rugged construction, low cogging torque and the capability of reluctance torque, so it is widely used in electric vehicle (EV). The research work deals with two control schemes, namely field oriented control (FOC) and direct torque control (DTC) are used in PMSM drive. A PMSM drive system based on field oriented control (FOC) & direct torque control (DTC) is designed and implemented for three–level diode clamped multilevel inverter (DCMLI) using Carrier based Pulse width modulation (CBSVPWM) techniques. The simulation of the field oriented control (FOC) & direct torque control (DTC) system of three–level diode clamped multilevel inverter (DCMLI) fed PMSM drive using MATLAB/Simulink and compared these two control schemes based on a PMSM used in hybrid electrical vehicle. In order to decrease current and torque ripple and fix switching frequency, a novel carrier based space vector modulation (CB-SVM) DTC scheme based on the control of stator flux, torque angle and torque was proposed. In carrier based space vector modulation (CB-SVM), the inverter output voltage is directly synthesized by the effective times and the voltage modulation task can be greatly simplified.

From the detailed comparison, direct torque control (DTC) based three-level diode clamped inverter fed PMSM drive has stood a feasible solution as compared to the field oriented control (FOC) control scheme in automotive application. Hence direct torque control (DTC) based Permanent Magnet Synchronous Motor drives can validated for hardware implementation.

A experimental implementation of direct torque control (DTC) based three level diode clamped multilevel inverter (DCMLI) fed PMSM drive using carrier based space vector modulation technique is proposed. In this proposed approach experimental work is carried out using AVR Microcontroller.

The proposed direct torque control (DTC) based three–level diode clamped multilevel inverter (DCMLI) fed PMSM drive is found acceptable because of its less distorted output, lower costs, better control performance and other advantageous features. The simulation & hardware results show that the proposed method can effectively suppress the torque ripple and improve driving performance for the PMSM drive. Hence it is used in automotive applications.

Problem Statement

The motor is normally fed from a 2- level VSI, which controls the torque and flux by using one of the two commonly accepted control strategies like, Field Oriented Control (FOC) and Direct Torque Control (DTC) independent of any variations in load parameters and disturbances. 3-level inverter when compared to conventional 2- level inverter has been widely used in medium to high power applications, due to lower harmonics of output voltage and current at same switching frequency with reduced voltage rating of power devices. Various modulation techniques have been developed to generate stepped output waveform in 3- level inverters. The existing PMSM drive used in automotive application comprised of three parts such as the PMSM motor, the two level voltage source inverter (VSI) and the processor.

The mythology used in existing Honda Civic2006 hybrid electrical vehicle model is namely, FOC and DTC with voltage selection strategy These two control strategies are compare on the basis of current, voltage, torque and speed. The main drawback of FOC is that it is implemented in the rotor flux reference frame and needs the continuous rotor position information to implement the coordinate transformation and suffer from current and torque ripples and variable switching frequency. Similarly in DTC, it is implemented in the stationary reference frame and doesn't need the continuous rotor position information except for the initial rotor position. However it controls the current, torque ripples and variable switching frequency up to some extent.

Hence a novel carrier based space vector pulse width modulation (CB-SVPWM) switching technique has been proposed for the DTC in Honda Civic 2006 hybrid electrical vehicle model which can decrease current ripple and fix the switching frequency. Following are the drawbacks of two level inverter in automotive application on the basis of simulation analysis.

1. High frequency switching is responsible for large switching losses.
2. Motor bearing failure and stator winding insulation breakdown problems occurs due to high dv/dt .
3. Electromagnetic interference (EMI) problems occur due to high frequency switching.
4. It has high current and torque ripples and variable switching.

To overcome these problems multilevel inverters is the alternative solution in automotive application.

Research Objectives and Contributions

The main objective of this research-work is enhancement of the performance of a Permanent Magnet Synchronous Motor (PMSM) drive in automotive application. In existing DTC method, proposed by some researcher using improved voltage vector selection strategy, has been used for switching. It has the drawback of current & torque ripples & variable switching frequency.

The objectives of the proposed work are:

i) Design & simulation of the Field Oriented Control (FOC) based three–level diode clamped multilevel inverter (DCMI) fed Permanent Magnet Synchronous Motor(PMSM) drive using novel carrier based space vector pulse width modulation(CB-SVPWM) technique.

ii) Design & simulation of the Direct torque control(DTC) based three–level diode clamped multilevel inverter (DCMI) fed Permanent Magnet Synchronous Motor(PMSM) drive using novel carrier based space vector pulse width modulation(CB-SVPWM) technique.

iii) To design and implement the lab setup for three–level diode clamped multilevel inverter (DCMI) fed PMSM drive using carrier based space vector pulse width modulation (CB-SVPWM) technique based on a AVR microcontroller.

iv) The performance of Permanent Magnet Synchronous Motor drive parameters such as speed, electromagnetic torque and motor current on basis of software and hardware implementation shall be carried out for automotive application.

v) To reduce the torque ripple, constant speed and constant switching frequency is maintained during entire simulation process.

The main contributions presented in this thesis are summarized as:

- In the first stage, a field oriented control of three level diode clamped Multilevel inverter (DCMLI) fed Permanent Magnet Synchronous motor is investigated. a closed loop controller is designed to obtain the desired output torque, speed and stator phase current of permanent magnet synchronous motor (PMSM) fed by a three level diode clamped inverter which is built using IGBT (Insulated gate bipolar transistor). Three modulation techniques

have been studied, Pulse Width Modulation (PWM), Space Vector Pulse Width Modulation (SVPWM) and a novel Carrier Based Space Vector Pulse Width Modulation (CBSVPWM). Simulation and analysis of the novel scheme is carried out by using MATLAB simulink model.

- In the second stage, a Direct torque control of three level diode clamped Multilevel inverter (DCMLI) fed Permanent Magnet Synchronous motor is investigated. A closed loop controller is designed to obtain the desired output torque, speed and stator phase current of permanent magnet synchronous motor (PMSM) fed by a three level diode clamped inverter which is built using IGBT (Insulated gate bipolar transistor). A Novel Carrier Based Space Vector Pulse Width Modulation (CBSVPWM) technique has been studied. Simulation and analysis of the novel scheme is carried out by using MATLAB simulink model. For the DTC using the switching table, current ripple is higher and the switching frequency of the VSI is also not constant. but it does not need the rotor position information except for the initial rotor position. A novel technology of carrier based space vector modulation (CB-SVM) is proposed for the DTC, which reduces current ripple and fix the switching frequency.
- In the third stage, performance of the field oriented control (FOC) and direct torque control (DTC) based Permanent Magnet Synchronous Motor drives are compared on basis of simulation result analysis. In the simulation analysis direct torque control(DTC) based Permanent Magnet Synchronous Motor drives can decrease current, torque ripples and fix the switching frequency as compared to field oriented control(FOC).Hence direct torque control(DTC) based Permanent Magnet Synchronous Motor drives can be validated for hardware implementation.
- In the fourth stage, an experimental implementation of three level diode clamped multilevel inverter (DCMLI) fed PMSM drive is proposed. In this proposed approach experimental work is carried out using AVR Microcontroller. In the experimental work, Atmega8 AVR Micro controller is used to generate the CBSVPWM pulses for three level diode clamped multilevel inverter (DCML) to drive the Permanent Magnet Synchronous Motor (PMSM).

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List of Abbrevations & Symbols

Abbreviations

PMSM	-	Permanent magnet synchronous motor
IPMSM	-	Interior permanent magnet synchronous motor
SPMSM	-	Surface permanent magnet synchronous motor
VSI	-	Voltage source inverter
SVM	-	Space vector modulator
PWM	-	Pulse width modulation
CBSVPWM	-	Carrier based space vector modulator
PWM - VSI	-	Voltage source inverter with PWM
DTC	-	Direct torque control
DTC-SVM	-	Direct torque control with space vector modulator
DTC -CBSVPWM	-	Direct torque control with carrier based space vector modulator
FOC	-	Field oriented control

Symbols

ω	-	Rotor Speed in electrical
N	-	Rotor Speed in Mechanical
Np	-	No. of Poles
TL	-	Load Torque
B	-	Friction Coefficient
J	-	Inertia of PMSM drive
R	-	Stator resistance.
V_d	-	Direct axis voltage.
Vq	-	Quadrature-axis voltage.
I_d	-	Direct axis current.
I_q	-	Quadrature-axis current.
L_d	-	Direct axis inductance.
L_q	-	Quadrature-axis. Inductance.
λf	-	Permanent magnet flux.
T_e	-	Electromagnetic torque.

CHAPTER – 1
INTRODUCTION

This chapter focuses on background history of PMSM in automotive application, classification of Permanent Magnet Synchronous Motor (PMSM) and its advantages. It also discusses Objectives of research work.

1.1. BACKGROUND

Electric motors (EMs) and generators are the primary workhorses in hybrid electric vehicles (HEVs). The generators convert mechanical power from the engine electrical power in order to charge the batteries and operate the motors. Motors produce the required torque to drive the wheels. There are many types of motors and generators used in HEVs: induction, switched reluctance, and permanent magnet. Each type requires the occurrence of a magnetic field. Reluctance and induction motors use an external source to provide the magnetic field, while the permanent magnet motors use permanent magnets for this purpose. The critical factors for these components are power, efficiency, controllability, cost, and durability [1-3].

Electric propulsion systems are the hearts of electric vehicle (EV).It consist of electric motors, power converters and electronic controllers [4]. As the Permanent Magnet Synchronous Motor (PMSM) can offer many advantages, including high power-to weight ratio, high efficiency, rugged construction, low cogging torque and the capability of the additional reluctance torque, it is widely used in the modern EV and hybrid EV. For the interior PMSM, there are two different high-performance control strategies, such as, the field oriented control (FOC) and the direct torque control (DTC). Both of them are widely used in the industry application. The FOC is implemented in the rotor flux reference frame and needs the continuous rotor position information to implement the coordinate transformation. The DTC is implemented in the stationary reference frame, doesn’t need the continuous rotor position information

except for the initial rotor position. But it suffers from high current and torque ripples and variable switching [5-11].

In order to decrease current and torque ripple and fix switching frequency, an improved DTC scheme based on the control of stator flux, torque angle and torque is proposed[12].This research work compares these two control strategies, FOC and DTC based on a surface mounted PMSM used in Honda Civic 2006 hybrid electrical vehicle. A novel technology of carrier based space vector modulation (CB-SVM) for the DTC, which can decrease current, torque ripples and fix the switching frequency, is propose and implemented on the same Honda Civic 2006 model.

This research work basically focuses on the design and analysis of FOC and DTC based surface mounted Permanent Magnet Synchronous Motor drives in Honda Civic 2006 hybrid electrical vehicle. The simulation of a FOC and direct torque control of PMSM is developed using MATLAB Simulink. The FOC and DTC is one of the high performance control strategies for AC machine. The main drawback of FOC is it needs the continuous rotor position information and the switching frequency of the VSI is not constant. The DTC scheme has been realized successfully in the Induction Motor drives. DTC technique is simple, robust and offers good dynamic performance. The main drawback of the DTC is its relatively high torque and flux ripples and also variable switching frequency in case of Induction motor. The performance of the Direct Torque Control of PMSM can be improved by reducing the high torque and flux ripples and maintaining a constant switching frequency using novel technology of carrier based space vector modulation (CB-SVM).The source to the variable switching frequency problem is the use of hysteresis comparators, in particular, the torque hysteresis comparator. Hence, a constant switching frequency torque controller should be designed to replace the conventional hysteresis-based controller in order to minimize the torque.

1.2 CLASSIFICATION OF PERMANENT MAGNET SYNCHRONOUS MOTORS (PMSM)

In PMSM, the electrically excited field winding synchronous motor can be replaced by permanent magnet (PM) [13]. The use of permanent magnets has many advantages including the elimination of brushes, slip rings, and rotor copper losses in the field winding. It leads to higher efficiency. Additionally since the copper and iron losses are concentrated in the stator, cooling of machines through the stator is more effective. The lack of field winding and higher efficiency results in reduction of the machine frame size and higher power/weight ratio.

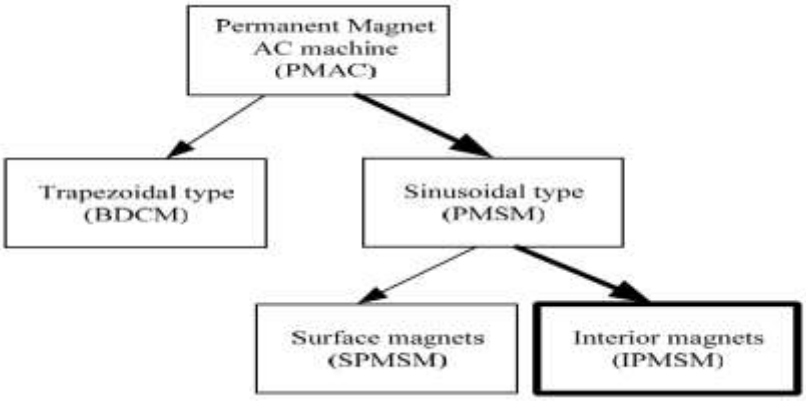

Fig. 1.1 : General Classification of AC synchronous motors.

(Source: www.isep.pw.edu.pl/icg/pdf/phd/dariusz_swierczynski.pdf)

Generally, the permanent magnet AC machines can be classified into two types (Fig.1.1.) such as, Trapezoidal type or “brushless DC machine” (BLDCM) and sinusoidal type called permanent magnet synchronous machine (PMSM). The BLDC machines operate with trapezoidal back electromagnetic force (EMF) and require rectangular stator phase current. The PMSM’s generated sinusoidal EMF and operate with sinusoidal stator phase current. The permanent magnet synchronous motors (PMSM) can be further divided into two main groups with respect to how the magnet bars are mounted in the rotor [14, 15]. In the first group magnets are mounted in the rotor this type is called Interior Permanent Magnet Synchronous Motors (IPMSM). The second group is represented by Surface Permanent Magnet Synchronous Motors (SPMSM). In the SPMSM magnet bars are mounted on the rotor surface.

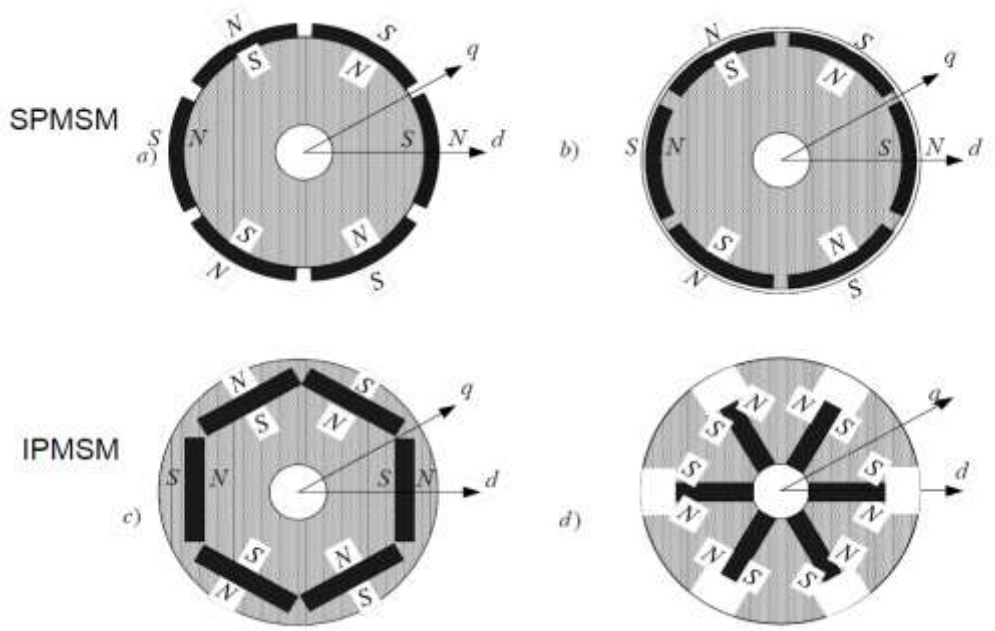

Fig. 1.2 : The cross section of the PMSM rotor shaft and the magnet bars placements: a),b),c) axial field direction, d) radial field direction.

(Source: www.isep.pw.edu.pl/icg/pdf/phd/dariusz_swierczynski.pdf)

The magnets can be placed in many ways on the rotor as shown in Fig. 1.2. In radial field fashion the magnet bars are along the radius of the machine and this arrangement provides the highest air gap flux density, but it has the drawback of lower structural integrity and mechanical robustness. Machines with this arrangement of magnets are not preferred for high-speed applications (higher than 3000 rpm). In axial field manner the magnets are placed parallel to the rotor shaft. This arrangement of magnets is much more robust mechanically as compared to surface-mounted machine. It makes possible to use IPMSM for higher-speed applications (contrary to SPMSM's).

Regardless of the fashion of mounting the permanent magnet (PM), the basic principle of motor control is the same and the differences are only in particularities. An important consequence of the method of mounting the rotor magnets is the difference in direct and quadrature axis inductance values. The direct axis reluctance is greater than the quadrature axis reluctance, because the effective air gap of the direct axis is multiple times that of the actual air gap seen by the quadrature axis. As

consequence of such an unequal reluctance, the quadrature inductance is higher than direct inductance $Lq > Ld$. It produces reluctance torque in addition to the mutual torque. Reluctance torque is produced due to the saliency in the quadrature and the direct axis magnetic paths. Mutual torque is produced due to the interaction of the magnet field and the stator current. In case where the magnets bars are mounted on the rotor surface the quadrature inductance is equal direct inductance $Ld = Lq$, because of the same flux paths in d and q axis, and as a result the reluctance torque disappears.

1.3 OBJECTIVES OF RESEARCH WORK

The main objective of this research-work is enhancement of the performance of a Permanent Magnet Synchronous Motor (PMSM) drive in automotive application. In existing DTC method, proposed by some researcher using improved voltage vector selection strategy, has been used for switching. It has the drawback of current & torque ripples & variable switching frequency.

The objectives of the proposed work are:

i) Design & simulation of the Field Oriented Control (FOC) based three–level diode clamped multilevel inverter (DCMI) fed Permanent Magnet Synchronous Motor(PMSM) drive using novel carrier based space vector pulse width modulation(CB-SVPWM) technique.

ii) Design & simulation of the Direct torque control(DTC)based three–level diode clamped multilevel inverter (DCMI) fed Permanent Magnet Synchronous Motor(PMSM) drive using novel carrier based space vector pulse width modulation(CB-SVPWM) technique.

iii) To design and implement the lab setup for three–level diode clamped multilevel inverter (DCMI) fed PMSM drive using carrier based space vector pulse width modulation (CB-SVPWM) technique based on a AVR microcontroller.

iv) The performance of Permanent Magnet Synchronous Motor drive parameters such as speed, electromagnetic torque and motor current on basis of software and hardware implementation shall be carried out for automotive application.

v) To reduce the torque ripple, constant speed and constant switching frequency is maintained during entire simulation process.

1.4 PROPOSED METHOLOGY OF PMSM DRIVE IN AUTOMOTIVE APPLICATION

1.4.1 Field Oriented Control (FOC)

This section deals with the description of the closed loop, field-oriented control of PMSM drive system which includes different components such as permanent magnet motors, position sensors, multilevel inverters and pulse width modulation(PWM),space vector pulse width modulation (SV-PWM) and carrier based space vector pulse width modulation(CB-SVPWM) controllers. The components are connected as shown in fig.1.3.

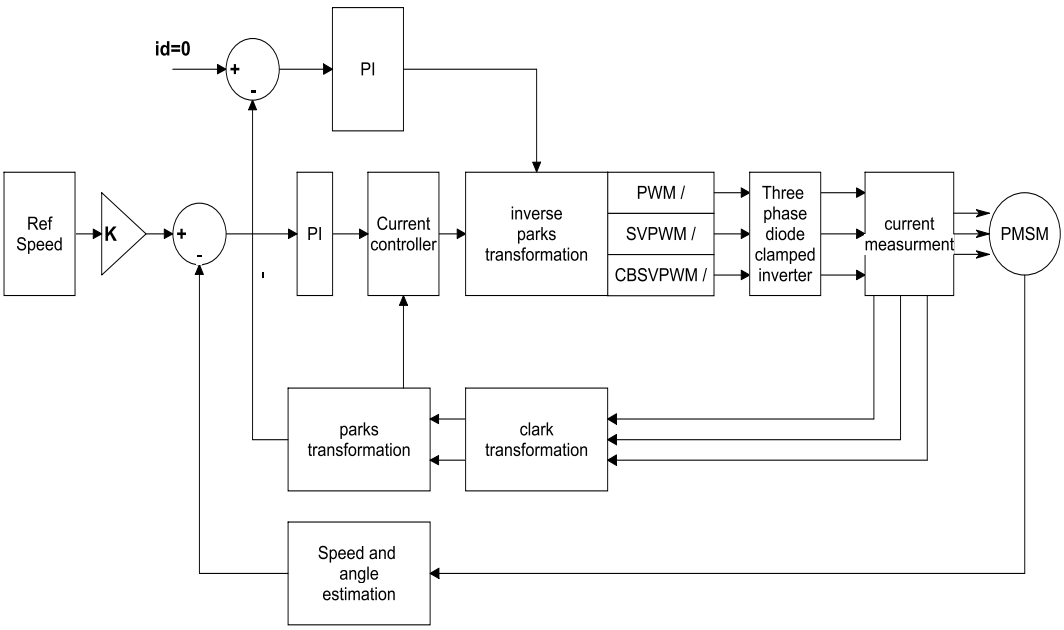

Fig.1.3 : Block diagram Field-Oriented Control of PMSM

The block diagram of closed loop PI control using Field Oriented Control (FOC) to investigate the speed and torque control with different modulation techniques such as pulse width modulation (PWM), space vector pulse width

modulation (SV-PWM) and carrier based space vector pulse width modulation (CB-SVPWM) for a voltage source three-level diode clamped inverter fed PMSM is shown in Fig1.3.The switch is used to carry out three modulation techniques. Block diagram of FOC of PMSM (Fig.1.3.) shows the reference waves which generated are compared with the triangular waves and the pulses which are obtained given to the 12 IGBT's of the three level diode clamped multilevel Inverter (DCMLI). The output of the inverter is given to the PMSM to control the speed and torque of the motor.

1.4.2 Direct torque control (DTC)

The basic principle in conventional DTC for PMSM is to directly select stator voltage vectors by means of a hysteresis stator flux and torque control as in Fig.1.4. From Fig.1.4. stator flux $\Psi_s^*$and torque $T_e^*$are compared by means of hysteresis band comparators. On the basis of the hysteresis comparators and stator flux sector a proper VSI voltage vector is selected by means of the switching table.

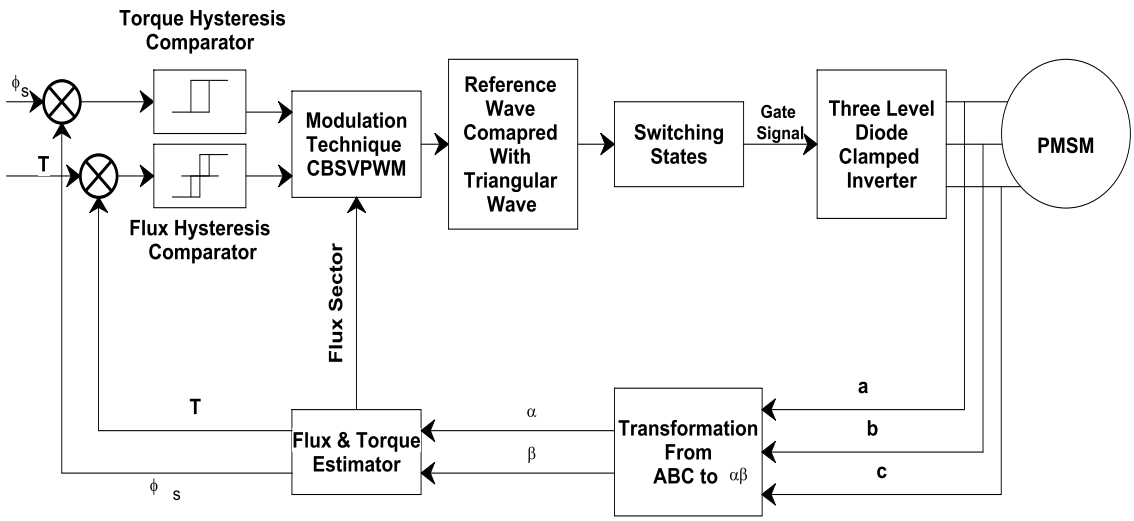

Fig.1.4 : Block Diagram of Direct Torque Control of PMSM

The main disadvantage of conventional DTC is high ripple levels in stator current, flux linkage and torque, due to the application of same active voltage vector during the whole sample period and possibly several consecutive sample intervals.

This can be overcome by using proper modulation technique which is a Space Vector Modulation (SVM) which synthesizes any voltage vector lying inside the sextant. In DTC-SVM the hysteresis comparators are replaced by an estimator which calculates an appropriate voltage vector to compensate for torque and flux errors. It gives good dynamic performance with less torque and flux ripple but introduces more complexity and looses an essential feature of DTC, its simplicity. To reduce the complexity involved in SVPWM, a novel modulation technique named Unified voltage modulation or carrier based space vector pulse width modulation (CBSVPWM) is described using the concept of effective time. By using this method the inverter output voltage is directly synthesized by the effective times and the voltage modulation task can be greatly simplified. The actual gating signals for each inverter arm can be easily deduced as a simple form using the effective time relocation algorithm. The block diagram of the DTC-CBSVPWM fed SPMSM using three-level diode clamped inverter is shown in Fig.1.4.The measured currents from the motor are transformed to α-β by using Clark transformation. The voltage is estimated from the inverter switching state and the DC-link voltage in the α-β reference frame.

1.5 DESCRIPTION OF THE PROPOSED LABORATORY TEST-STAND

The basic structure of laboratory setup is presented in Fig.1.5. The laboratory setup consists of rectifier circuit, diode clamped multi level inverter (DCMLI), Permanent Magnet Synchronous Motor, AVR Microcontroller, Hall-effect sensor, current sensor and Mechanical loading arrangement which is used as a load. The PMSM machine is supplied by CB-SVPWM inverter, which is controlled by AVR Microcontroller. In AVR Microcontroller Atmega8 is used for switching purpose & Atmega16 is used for monitor &control. The three level diode clamped multilevel inverter is supplied from single-phase diodes rectifier. The design of the system is done for variable frequency operation of the PMSM drive using AVR Microcontroller for the different circuits which are given below.

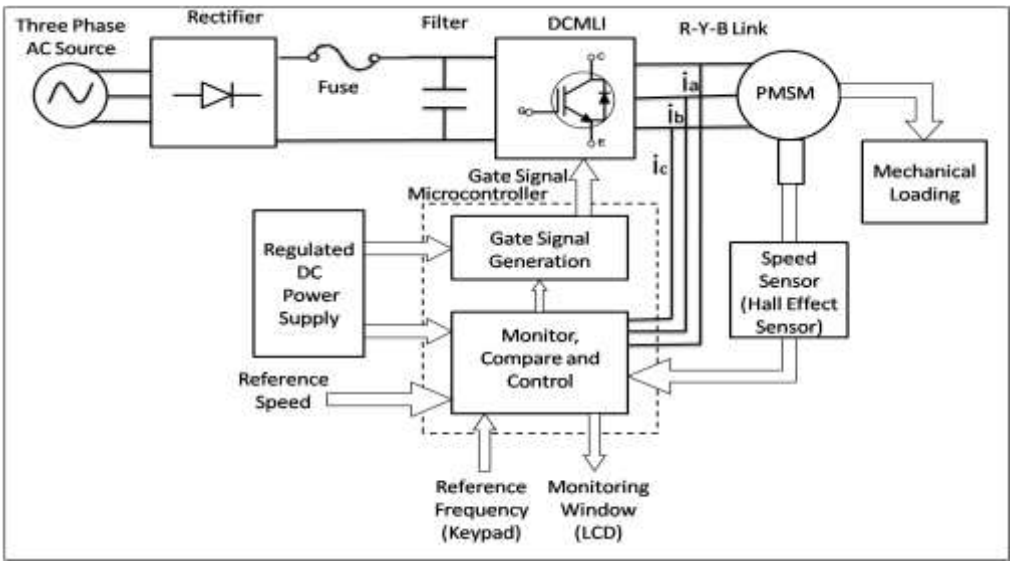

Fig.1.5 : Block Diagram of Hardware Implementation

1.6 SCIENTIFIC CONTRIBUTIONS

The main contributions presented in this thesis are summarized as:

- In the first stage, a field oriented control of three level diode clamped Multilevel inverter (DCMLI) fed Permanent Magnet Synchronous motor is investigated. a closed loop controller is designed to obtain the desired output torque, speed and stator phase current of permanent magnet synchronous motor (PMSM) fed by a three level diode clamped inverter which is built using IGBT (Insulated gate bipolar transistor). Three modulation techniques have been studied, Pulse Width Modulation (PWM), Space Vector Pulse Width Modulation (SVPWM) and a novel Carrier Based Space Vector Pulse Width Modulation (CBSVPWM). Simulation and analysis of the novel scheme is carried out by using MATLAB simulink model.

- In the second stage, a Direct torque control of three level diode clamped multilevel inverter (DCMLI) fed Permanent Magnet Synchronous motor is investigated. A closed loop controller is designed to obtain the desired output torque, speed and stator phase current of permanent magnet synchronous motor (PMSM) fed by a three level diode clamped inverter which is built using IGBT (Insulated gate bipolar transistor). A Novel Carrier Based Space Vector Pulse Width Modulation (CBSVPWM) technique has been studied.

Simulation and analysis of the novel scheme is carried out by using MATLAB simulink model. For the DTC using the switching table, current ripple is higher and the switching frequency of the VSI is also not constant. but it does not need the rotor position information except for the initial rotor position. A novel technology of carrier based space vector modulation (CB-SVM) is proposed for the DTC, which reduces current ripple and fix the switching frequency.

- In the third stage, performance of the field oriented control (FOC) and Direct torque control (DTC) based Permanent Magnet Synchronous Motor drives are compared on basis of software result analysis. In the software analysis direct torque control(DTC) based Permanent Magnet Synchronous Motor drives can decrease current,torque ripples and fix the switching frequency as compared to field oriented control(FOC).Hence direct torque control(DTC) based Permanent Magnet Synchronous Motor drives can be validated for hardware implementation.
- In the fourth stage, an experimental implementation of three level diode clamped multilevel inverter (DCMLI) fed PMSM drive is proposed. In this proposed approach experimental work is carried out using AVR Microcontroller. In the experimental work, Atmega8 AVR Micro controller is used to generate the CBSVPWM pulses for three level diode clamped multilevel inverter (DCML) to drive the Permanent Magnet Synchronous Motor (PMSM).

Chapter 2 deals with literature survey on modeling, analysis and simulation of PMSM drives in automotive application.

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CHAPTER– 2
LITERATURE SURVEY

This chapter focuses on pre- research literature review & ongoing references during the span of research work. It also discusses the various research papers in area of Permanent Magnet Synchronous Motor (PMSM) drives & their control techniques.

2.1 SURVEY OF AC MOTORS

The advantages of induction motor (IM), is simple construction, reliability, ruggedness, and low cost. IM has found very wide industrial applications. Furthermore, in contrast to the commutation dc motor, it can be used in an aggressive or volatile environment since there are no problems with spark and corrosion. These advantages, however, are superseded by control problems when using an IM in industrial drives with high performance demands. This is where the Permanent Magnet Synchronous Motor (PMSM) comes in, because it serves very well for high performance vehicular applications (especially on-road commercial cars) where a driver is more concerned about factors such as efficiency, speed, reliability and acceleration. The PMSM is a rotating electric machine where the stator is a classic three-phase stator like that of an induction motor and the rotor has surface-mounted permanent magnets. In PMSMs there is no stator power dedicated to the magnetic field production.

2.1.1 Permanent Magnet Synchronous Motor

PMSMs have a variety of applications in many areas such as automobiles, robotics, traction, and aerospace technology. PMSMs have extensive automotive applications due to their high efficiency, low inertia and high torque-to-volume ratio and this is due to its several advantages like high efficiency, compactness, fast dynamics and high torque to inertia ratio.

2.2 RESEARCH BACKGROUND

Permanent magnet motor drives have been an area of interest for the past thirty years. Different researches have carried out modeling, analysis and simulation

of PMSM drives. This content offers a brief review of some of the published work on the PMSM drive system.

- The original concept of DTC was proposed by Takahashi and Noguchi in 1986 for application in Induction Motors. Their idea was to control the stator flux linkage and the torque directly, not via controlling the stator current. This was accomplished by controlling the power switches directly using the outputs of hysteresis comparators for the torque and the modulus of the stator flux linkage and selecting an appropriate voltage vector from a predefined switching table. The table was called the 'optimum switching table". The measurement of the rotor angle was not used. [16, 17]
- Same kind of control was proposed by Depenbrock (1987). At first, Takahashi and Noguchi did not give any name to their new control principle. In a later paper Takahasi and Ohmori (1987) named the control system as direct torque control, DTC. Depenbrock called his control method Direct Self Control, DSC. Tiitenen et al discussed the first industrial application of the DTC. After that,number of papers on the DTC has grown tremendously on different aspects of the DTC for asynchronous motors. In recent years there has been interest to apply the DTC to permanent magnet synchronous motors. [18]
- L.Zhong et al discussed the implementation of DTC in PMSM Drives. In 1998, Rahman et al proposed a DTC scheme for a wide speed range operation of an interior PMSM drive. The proposed scheme possesses some attractive features compared to the conventional current-controlled drives like field oriented control (FOC). Later on, Tang et al proposed a DTC control schemes for the IPM featuring almost fixed switching frequency. [19,20, 21]
- In 2002, Rahman et al, proposed a completely sensor less DTC control for an IPM drive, which uses a new speed estimator from the stator flux linkage vector and the torque angle. To reduce the torque ripples, Sun et al proposed a fuzzy logic algorithm to refine the selection of the voltage vectors. Today, the DTC has become an accepted control method beside the field oriented control. [22,23]

- Direct torque control was proposed by M. Depenbrock and I. Takahashi for the induction motor drive in the middle of 1980s. The basic idea of DTC is to control the torque and flux linkage by selecting one of the voltage vectors generated by a VSI in order to maintain flux and torque within the limits of two hysteresis bands. The right selection of the vector voltage allows a decoupled control of flux and torque without d-q coordinate transformation, PWM and PI current regulators that Field Oriented Control (FOC) usually need. DTC offers many advantages such as lower parameter dependency and complexity compared with the FOC, which makes the system more robust and easier to implement[24].
- In 1989,Pillay and Krishnan, R. presented the vector control as well as complete modeling of the drive system in rotor reference frame except damper windings. [25]
- In 1998, M.R. Zolghadri, J. Guiraud, J. Davoine, D. lRoye presented two flux estimators which are studied for a sensoreless direct torque controlled permanent magnet synchronous motor drive. Some simulation and experimental results are presented. These results show that direct torque control can be used with some restrictions for sensorless permanent magnet synchronous motor drives.[26]
- In 1999, the fuzzy logic based speed control of an interior permanent synchronous motor (IPMSM) drive was presented by M. N. Uddin and M. A. Rahman. The fundamentals of fuzzy logic algorithms related to motor control applications were explained. A new fuzzy speed control algorithm for IPMSM drive has been designed. [27]
- In 2005, Yan Deng, Hongyan Wang, Chao Zhang, Lei Hu, Xiangning He. Presented Multilevel PWM Methods Based On Control Degrees Of Freedom Combination and Its theoretical analysis. Diode clamped multilevel inverter is chosen for feeding PMSM drive over all configurations of multilevel inverter. By using the proposed topology the number of switches are reduced and hence the efficiency is improved as in [28]

- In 2008, M. S. Merzoug, and F. Naceri presented main characteristics of field-oriented and direct torque control schemes for PMSM drives.They are studied the simulation with a view to highlighting the advantages and disadvantages of each approach. It is difficult to clearly state on the superiority of DTC versus FOC because of the balance of the merits of the two schemes.[29]
- In 2010,Zhonghui Zhang, Jiao Shu simulated the field oriented vector control of PMSM drive using current reference tracking and PWM inverter switchingThis work used conventional PI controller for tracking purpose. [30]
- In 2010, A. El Shahat & H. El Shewy presented a detailed Simulink model for a PMSM drive system with field oriented control which was developed and operated at and above rated speed using two current control schemes. A comparative study has been made of the two current control schemes. A speed controller has been designed successfully for closed loop operation of the PMSM drive system so that the motor runs at the commanded or reference speed. All the results are well depicted if compared with any previous contributions in the literature.[31]
- In 2010, Yaohua Li, Dieter Gerling, Jian Ma, Jingyu Liu, Qiang Yu presented a comparison of the experimental results of the interior PMSM drive used in the electric vehicle under the control of the different control strategies, Such as FOC, DTC. Comparing with the switching table, the voltage vector selection strategy proposed can decrease current and torque ripple and fix switching frequency.[32]
- In 2011, Li Yaohua, Ma Jian, Yu Qiang, Liu Jiangyu presented a voltage vector selection strategy which uses stator flux position and torque angle information to determine the applied voltage vector and uses SVM to generate it. Simulation and experimental results prove the proposed voltage vector selection strategy can decrease stator current and torque ripples and fix switching frequency compared with switching table.[33]

- In 2011, Li Yaohua, Liu Jingyu, Ma Jian, Yu Qiang presented a simplified voltage vector selection strategy for the tested PMSM, where the SVM is used to generate the applying voltage vector. Experimental results show voltage vector selection strategy can decrease stator current and torque ripples and fixes the switching frequency compared with switching table.[34]
- In 2012, L.M. Masisi ,S. Williamson, & P. Pillay presented comparsion of 2-level and 3-level inverters.They were compared based on the copper losses and the torque ripples at particular switching frequencies. The 3-level inverter on average promised much lower copper losses and torque ripples as compared to the 2-level inverter.The results also reveal that there might be a compromise between torque ripples and copper losses at particular switching frequencies. It was also evident that the losses depend not only on motor speed but also on the switching frequency and the choice of the inverter.[35]
- In 2012, Narayan Prasad Gupta &Preeti Gupta presented the simulink model of proposed Direct Torque Control for PMSM drive which has been developed and analyzed. With sensing of three phase stator voltages, this technique will be most reliable and promising with reduced cost. Space vector pulse width modulation techniques have been used for six gate pulse generation of three phase bridge inverter. A number of simulation results shows that DTC scheme has fast and smooth dynamic response of torque and stator flux linkage followed by excellent performance against sudden change in speed and torque.[36]
- In 2012, Xu Wang, Yan Xing, Zhipeng He, Yan Liu presented new direct torque control algorithm of PMSM by using SVPWM. The dynamic and static performance of the control system is better than the conventional DTC system of PMSM. Simulation results indicate that the proposed SVM-DTC can reduce the flux and torque ripple efficiently, and has quicker dynamic response and less current harmonic comparing with the conventional DTC.[37]
- In 2013, P.Ramana, B.Santhosh Kumar, Dr.K.Alice Mary, Dr.M.Surya Kalavathi presented a method for PMSM drive based on FOC using SVPWM,

SPWM and Third Harmonic Injection PWM. Several numerical simulations using MATLAB-Simulink have been carried out in steady-state and transient-state. According to the results, the proposed technique is able to reduce torque ripple, speed error, and time to reach transient-state at abrupt mechanical load changes. In addition, we could have some other advantages like, constant switching frequency, fast transient response, and tunable output torque and speed with lower error.[38]

- In 2013, Harikrishna Raj Pinkymol,,Ali Iftekhar Maswood &,Aditya Venkataraman presented a SVPWM scheme for 3-level NPC inverter for Permanent magnet synchronous motor drive. Switching vectors and optimum switching sequence are generated to improve the efficiency of the motor drive system. The neutral point unbalance in 3-level NPC inverter is nullified by changing the switching sequence and rearranging the duty ratio of redundant vectors. The detailed analysis investigates dc link capacitor voltage control and the SVPWM technique.[39]
- In 2013, G. Sree Lakshmi, S. Kamakshaiah & G. Tulasi Ram Das presented the simulation model of closed loop control of three-level diode clamped inverter fed IPMSM drive using three different modulation techniques. The output voltage, current of the inverter and the speed, torque and the three-phase currents of the IPMSM for SPWM, SVPWM and CBSVPWM have plotted. From the analysis we can conclude that the CBSVPWM is similar to SVPWM but much simple, easy and the fastest method without much mathematical calculations like angle and sector determination as in SVPWM. This method can be easily extended to n-level inverter. THD of voltage and current also reduces with CBSVPWM.[40]
- In 2014, M.Haris, Dr.M.K.Pathak & Dr.Pramod Agarwal presented two-level and multilevel inverter fed PMSM drive with Sinusoidal PWM technique is analyzed. The simulation results show that PMSM drive performance had been improved with multilevel inverter fed topology. The MLI fed system has better torque performance, lesser torque ripple and better speed response compared with conventional 2-level PWM inverter.[41]

- In 2014, V.S. Bharath, Gopinath Mani presented the simulation of multilevel inverter and closed loop multilevel inverter fed drives using MATLAB/SIMULINK software. Closed loop models are developed and they are used successfully for simulation. The simulation studies indicate that a simple way to get the desired output voltage with minimum THD. The simulation results are in line with the predictions.[42]

2.3 REVIEW

Research work related to Permanent Magnet Synchronous Motor drive in automotive application were studied and reviewed.

Following are the highlights of the review.

- Vector control is the most important, simple and efficient method to control the Permanent Magnet Synchronous Motor, which can be divided into two types. FOC and DTC. The main objective in FOC is to control the current vector and in DTC the main objective is to control the torque producing flux vector.In the middle of 1980's Takahashi and Depenbrock proposed DTC for induction machines and in the late 1990 French and Zhong which was then applied to PMSM. The direct torque control (DTC) is an accurate controller for PMSM which is based on decoupled control of flux and torque which achieves robust and fast torque response in transient and steady-state operating condition, without the need of current regulators, speed or position sensors, PWM signal generator and coordinate transformation. DTC has many advantages over current control. However it has some disadvantages such as variable switching frequency ,high current ripples, and difficulty in controlling torque and flux.
- In recent years, above problem has been overcome by the development of multilevel inverter proposed by Martins and Vas, A smoother torque can be expected with more voltage space vectors available to control flux and torque. However, more power devices are needed to achieve a lower ripple and almost constant switching frequency which is obtained by using proper modulation techniques. Modified DTC schemes with low torque ripple and constant

switching frequency were reported by others, where SVM is implemented along with DTC, so as to provide a constant inverter switching frequency. SVPWM gives good performance, but however the complexity involved is more in calculating angle and sector.

- For the reduction of the complexity involved in SVPWM, a novel modulation technique named CBSVPWM is described using the concept of effective time. Thus by using the above method the inverter output voltage is directly synthesis by the effective times and the voltage modulation task can be greatly simplified. The gating signals for each inverter arm can be easily deduced as a simple form by using effective time relocation algorithm. In this research work a DTC-CBSVPWM is analyzed with surface-mounted permanent magnet synchronous motor and the torque and speed response is studied by using three-level diode clamped inverter.

Chapter 3 deals with mathematical modeling, torque equation & equivalent circuit of Permanent Magnet Synchronous Motor (PMSM)

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CHAPTER– 3

THE MATHEMATICAL MODEL OF PMSM

This chapter focuses on the modeling of PMSM in rotor reference frame; electromagnetic torque equation for PMSM with pole saliency has been derived. The per-phase equivalent circuit of Permanent Magnet Synchronous Motor is drawn & also explain phasor diagram of PMSM without field-weakening & with field-weakening.

3.1 INTRODUCTION

The present chapter deals with the modeling of Permanent Magnet Synchronous Motor (PMSM) in the 'dq' rotating reference frame and applying this model for deriving the torque equation of the machine. The per-phase equivalent circuits with and without field weakening are presented along with the relevant equations. Closed-loop control of Permanent Magnet Synchronous Motor with field-oriented control and direct torque control technique is presented and the same approach has been used for the research work.

3.1.1 Modeling of PMSM in rotor reference frame

The modeling of PMSM machine has been presented henceforth in the rotor reference frame. In a PMSM, the rotor is a permanent magnet without any windings and hence there are no equations associated with the rotor [2]. The 3-φ stationary 'abc' frame can be transformed into 2-φ synchronously rotating 'dq' frame, with the help of abc → dq transformations. In the 'dq' frame, stator has two windings: d-axis winding and q-axis winding; and the d-axis winding is aligned with the magnetic pole axis. Consider the PMSM machine running at the speed of 'ω_r', in anti-clockwise direction, as shown in Fig.3.1.

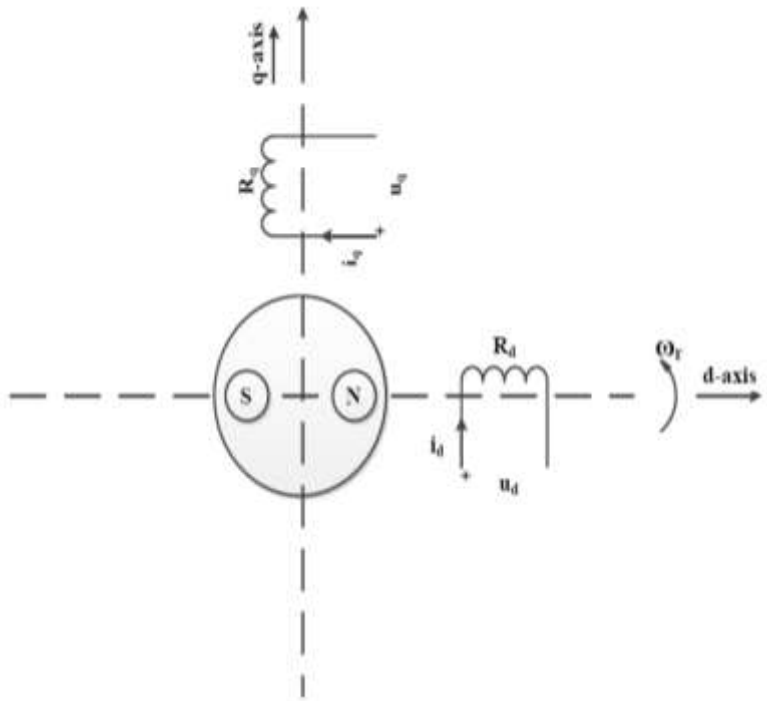

Fig. 3.1 : Model of PMSM in 'dq' or Rotor Reference Frame

(Source:Spectrum.library.concordia.ca/975146/1/Sejpal_MASc_S2013.pdf)

From Fig.3.1, the voltage induced in the d-axis winding is given by:

$$u_d = R_d i_d + \frac{d\lambda_d}{dt} - \omega_r \lambda_q \tag{3.1}$$

Where, 'R_d' and *'i_d'* are the d-axis stator resistance and current and the voltage induced in the q-axis winding is given by:

$$u_q = R_q i_q + \frac{d\lambda_q}{dt} - \omega_r \lambda_d \tag{3.2}$$

Where, 'R_q' and 'i_q' are the q-axis stator resistance and current

The terms *'$\omega_r \lambda_q$'* and *'$\omega_r \lambda_d$'* represent the rotationally induced EMF in the stator due to the rotation of the *'dq'* reference frame at the speed 'ω_r'.

Where,

$$\lambda_d = L_d i_d + \lambda_m \tag{3.3}$$

λ_d = flux-linkage in the d-axis stator (Wb)

λ_m is the permanent magnet rotor flux as the d-axis is aligned along the rotor NS-magnetic axis and,

$$\lambda_q = L_q i_q \tag{3.4}$$

λ_q = *flux-linkage in the q-axis stator (Wb)*

λ_m is absent in this case as there are no magnets along the q-axis

In the present study, a round rotor PMSM is considered and in this case the d-axis and qaxis inductance values are equal.

$$L_d = L_q \tag{3.5}$$

3.1.2 Torque equation of Permanent Magnet Synchronous Motor

The torque equation for PMSM is given by: [43]

$$T_e = \frac{3}{2}\frac{p}{2}(\lambda_d i_q - \lambda_q i_d) \tag{3.6}$$

Substituting for *'λd'* and *'λq'* in the torque equation of PMSM,

$$T_e = \frac{3}{2}\frac{p}{2}[(\lambda_d i_d + \lambda_m) i_q - L_q i_q i_d] \tag{3.7}$$

$$T_e = \frac{3}{2}\frac{p}{2}[(L_d - L_q) i_d i_q + \lambda_m i_q] \tag{3.8}$$

It can be seen that the torque developed in a PMSM consists of two components given by:

$$Reluctance\ torque = \frac{3}{2}\frac{p}{2}(L_d - L_q) i_d i_q \tag{3.9}$$

$$field\ torque = \frac{3}{2}\frac{p}{2}\lambda_m i_q \tag{3.10}$$

Since, for the round-rotor PMSM under consideration, the *d* and *q*-axes inductances values are equal, i.e., Ld , Lq, the reluctance torque component caused by the difference between the d-axis and q-axis inductances, gets vanished.

$$T_e = \frac{3}{2}\frac{p}{2}\lambda_m i_q \tag{3.11}$$

Hence the electromagnetic torque present in a round rotor permanent magnet synchronous machine is nothing but the field torque which is present due to the permanent magnet flux linkage, λm. For a chosen permanent magnet synchronous

machine, the number of poles (p) is constant and also the permanent magnet rotor flux-linkage *(λm).* Hence, the electromagnetic torque equation for the round-rotor PMSM can be re-written as

$$T_e = Kt\, i_q \tag{3.12}$$

Where, K_t = Torque constant

$$K_t = \frac{3}{2}\frac{p}{2}\lambda_m \tag{3.13}$$

Therefore, the q-axis component of stator current is also called the torque-producing component of current. It is known that the electro-magnetic torque of the motor should balance the torque as a result of the applied load, the viscous friction (B) and the moment of inertia (J) of the motor. Therefore, electro-magnetic torque can be expressed as

$$T_e = T_l + B\,\omega_m + J\,\frac{d\omega_m}{dt} \tag{3.14}$$

ω_m = mechanical speed of the rotor

ω_r = electrical speed of the rotor

The above equations can be used as the basis for modeling the transient and steady-state response of the PMSM under consideration. When this motor is started from stalled (rest) condition and also when acceleration is required, high torque needs to be applied due to its high inertia. In order that the rotor of the machine rotates at the desired speed, appropriate acceleration is desirable. The high torque in turn will demand high in-rush current. Once the speed starts building up from the initial condition, the initial high torque that was required can slowly be reduced once the motor has accumulated a good speed. Apart from this, by virtue of increasing speed, the back Electro-Motive Force (EMF) of the Permanent Magnet Synchronous Motor (PMSM) also starts increasing. Then, a point reaches where for a given strength of the magnetic field, or the rotor magnetic flux, a base speed is reached where the input (or the external) voltage cannot push anymore current into the electric motor against the developed back EMF of the machine. It is because the sum of the back EMF and the voltage drop across the stator impedance of the machine gets equal to the input voltage thus barring the flow of current from the output of the inverter towards the machine.

3.1.3 Per-phase equivalent circuit of Permanent Magnet Synchronous Motor

The single-phase equivalent circuit of a permanent magnet synchronous machine [44] can be demonstrated as in Fig.3.2. The per-phase resistance (*R*) and per-phase inductive reactance (X_L) are shown and the Back EMF is given as *E*.

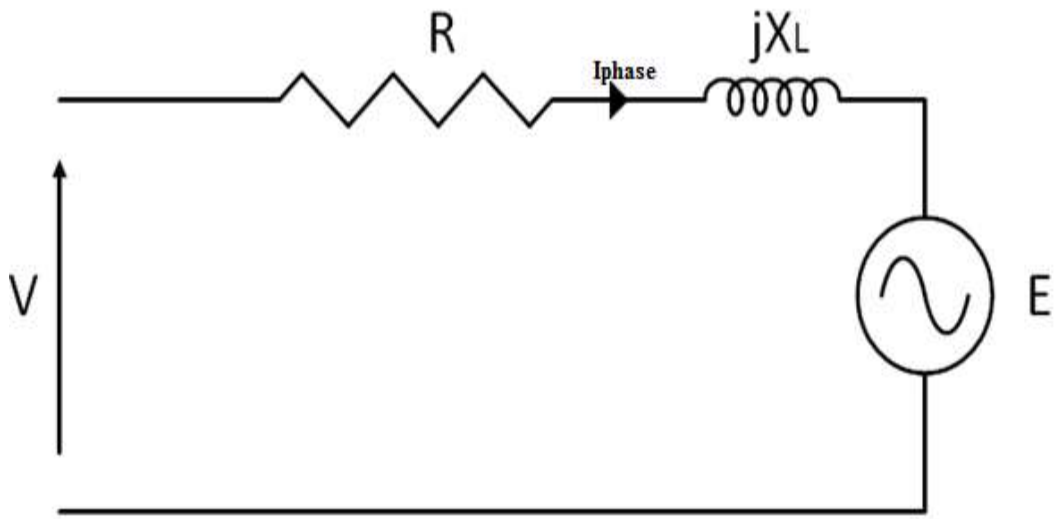

Fig. 3.2 : Per-phase Equivalent Circuit of a Permanent Magnet Synchronous Machine

The stator current (*I*) is composed of two components: the torque-producing component (I_q) and the flux-producing component (I_f) in the direction of the permanent magnet flux of the rotor (λ). The angle between the stator phase current and the flux vector is the torque angle (δ). The power factor angle (Φ) is the angle between the terminal voltage (*V*) and the stator phase current.

3.1.4 Phasor diagram of PMSM without field-weakening

The phasor diagram of the permanent magnet synchronous machine [45] can be realized as shown in Fig.3.3. Since the voltage drop across the impedance is a function of the current, it might not be possible to further increase the current or the torque due to the limited voltage output of the inverter. In order to avoid such a situation, it is important to weaken the back EMF with increasing speed. In case of a PMSM, it is done by introducing flux-weakening wherein the rotor magnetic field is

weakened in order to lower the back EMF voltage that is induced in the stator winding.

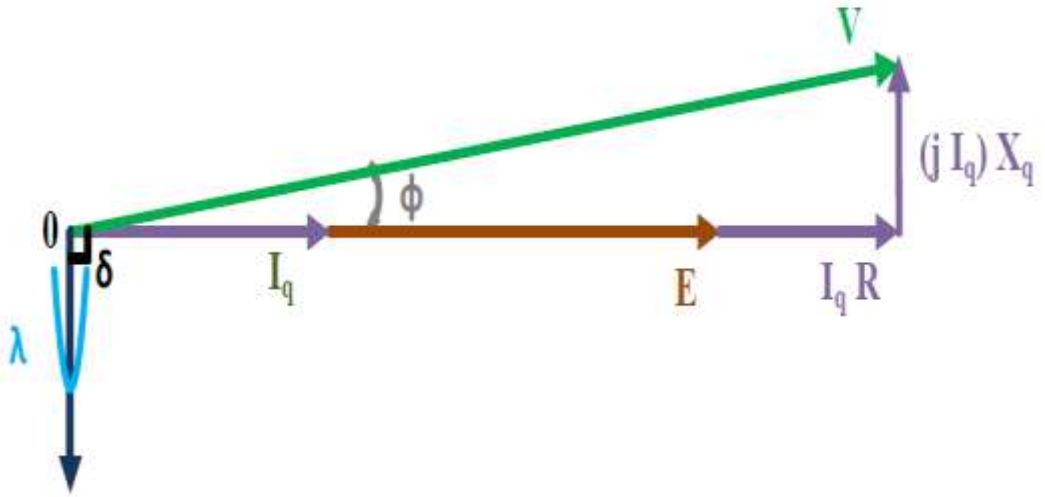

Fig. 3.3 : Phasor Diagram of Single-Phase of PMSM before Introducing Field- Weakening

(Source:pectrum.library.concordia.ca/975146/1/Sejpal_MASc_S2013.pdf)

Field weakening requires an opposing magnetic field to be applied to the permanent magnets. The fundamental approach behind flux-weakening control is to introduce and increase the magnitude of "opposing" current and employ the concept of armature reaction (as in DC motors) so as to reduce the air-gap flux thereby reducing the effective permanent magnet flux. This approach affects the torque-component of current (and in turn, the torque) for the same value of stator current.

3.1.5 Phasor diagram of PMSM with field-weakening

In order to weaken this permanent magnet flux which is constant, current *Id* which produces a flux, in the direction opposing the permanent magnet flux, is injected and this component of current is termed as the flux-weakening component of current (*Id*). The voltage drop across the inductive reactance (*jIdXd*) opposes the direction of back EMF thus reducing its effect; as shown in the phasor diagram of Fig.3.4.

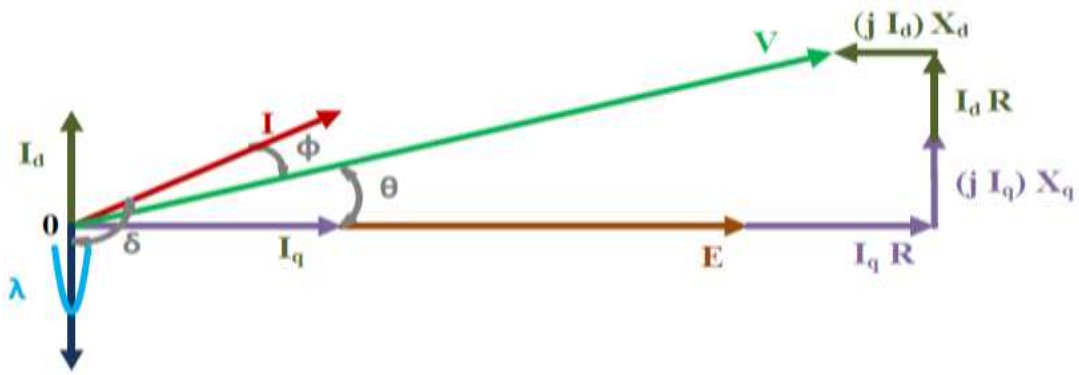

Fig. 3.4 : Phasor Diagram of Single-Phase of PMSM after Introducing Field- Weakening

(source:pectrum.library.concordia.ca/975146/1/Sejpal_MASc_S2013.pdf)

Using the Pythagorean Theorem for the phasor diagram in Figure 3.4,

$$V = \sqrt{(E + I_q R - I_d X_d)^2 + (I_d R + I_q X_q)^2} \quad (3.15)$$

When there is no field-weakening employed, $I_d = 0$ is substituted for above Equation (3.8); and the corresponding phasor diagram is as demonstrated in Fig. 3.3. The load power factor is given by '*cos φ*' and the power factor angle '*φ*' can be evaluated

$$\Phi = \delta - \theta$$

Where,

$$\theta = \textit{the rotor angle}$$

When there is no field-weakening,

$$\delta = л/2$$

When field-weakening is applied,

$$\delta > л/2$$

Where= $\tan^{-1}(I_q/I_d)$

$$\theta = tan^{-1}\left\{\frac{I_d R + I_q X_q}{E + I_q R - I_d X_d}\right\} \quad (3.16)$$

For the same amount of output current, when a certain amount of flux-weakening component of current is injected, the torque-producing component of current decreases and thus reduces the torque requirement, as shown in Fig.3.5. The inverter that drives the motor has limitations with respect to the voltage rating such that the stator voltage supplied to the motor from the inverter is limited by virtue of the DC-link voltage, thus limiting the speed (*N*) at which the motor can run; and the current rating such that the absolute value of stator current is required to be maintained below the maximum limit dictated by the maximum current rating of the inverter. The torque-producing component of current (*Iq*) can be set up to the maximum limit in the normal operating range and the flux-producing component (*Id*) can be set to zero to achieve maximum efficiency of PMSM. However, there is a limit on the absolute current value due to which the torque-producing current component is limited, in the field weakening range. The limit for the torque-producing current component is given as in eq.3.10.

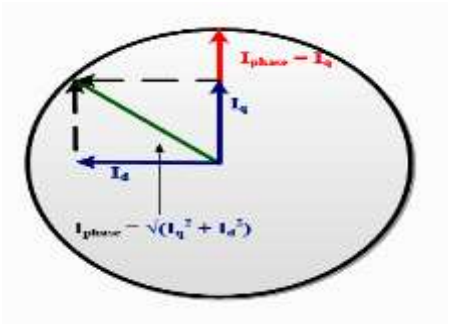

Fig. 3.5 : Torque and Flux-Producing Components of the Stator Phase Current
(source:pectrum.library.concordia.ca/975146/1/Sejpal_MASc_S2013.pdf)

$$I_q < \sqrt{(I_{phase}^2 - I_d^2)} \tag{3.17}$$

This function can be incorporated by introducing a field-weakening controller which springs into action whenever the stator voltage approaches to exceed the maximum voltage limit of the inverter. This controller introduces a negative value of the flux producing component so that the above inequality is satisfied. Flux-weakening helps weaken the constant permanent magnet rotor flux and thus allows the motor to run at an extended speed range. Up to the base speed, the motor is run at

rated flux-linkage (λ) value of the rotor where V/f control is followed (as per the nomenclature, '*V*' denotes the induced EMF in the stator and '*f*' denotes the stator frequency); as speed is related to frequency as shown in equation:

$$N = \frac{120f}{p} \tag{3.18}$$

Alternatively, the fundamental frequency of the output voltage and current of the inverter, going into the machine can be given by:

$$f = \frac{pN}{120} \tag{3.19}$$

N = Speed of the machine (RPM)

f = Stator electrical frequency (Hz)

p = Number of poles

Flux-weakening can be related to the increase of speed and can be summarized as follows. Beyond the base speed, the back EMF also increases as it is a function of speed. Since the inverter is a voltage source inverter with constant DC input voltage, the inverter cannot supply enough voltage to spin the machine in motoring mode beyond the base speed, overcoming the back EMF. Hence, it is required to weaken the field flux for the machine to be able to run in motoring mode beyond the base speed. By doing so, the back EMF is weakened for higher speed values thus resulting in the reduced V/f ratio (as the back EMF decreases and frequency increases; in-turn, speed

$$X_s = 2\pi f L_s \tag{3.20}$$

From the maximum power rating and the maximum back EMF of the machine, one can determine the maximum current rating of the machine given by:

$$P_{max} = 3E_{LLmax}I_{max} \tag{3.21}$$

From the above equation, one can obtain the maximum current value, I_{max}. Now, depending on the value of speed, one can determine the value of current for that particular speed condition. If this calculated value of phase current is greater than the maximum value of current, I_{max}, the current value is limited to I_{max}, otherwise, the obtained value of phase current is used for calculation. For the present study, a PMSM

which is used in the automotive industry with the following ratings has been considered:

The values of the PMSM under consideration are as shown in Table 3.1.

Table 3.1 : Parameters of the Permanent Magnet Synchronous Motor

Parameter	Value
R- Stator resistance	1.6 Ω
L_d-- direct axis inductance	0.006365 H
L_q - quadrature-axis. Inductance	0.006365H
P- No of pole pair	2
λf - permanent magnet flux	0.1852 Wb
F –Viscous coeiffient	0.00005396Nm-s
J –Movement of inertia	0.0001854 Kgm^2

For the PMSM chosen, there are two regions of operation, the transient region (at starting and during accelerations) and the permanent or continuous region (under steady-state of operation). Also, the PMSM operates in the following two speed ranges:

- Normal Range of Operation in which the speed of the motor is below its base speed. This range of operation signifies the Constant Torque condition.
- Extended Range of Operation, i.e. the Field-Weakening Range of Operation, in which the motor is required to be run beyond its base speed. This range of operation signifies the Constant Power condition. This can be depicted as shown in Fig.3.6. and Fig.3.7.where the Transient Region and the Continuous Regions of Operation have been demonstrated respectively. The required line-to-line voltage to run the PMSM is supplied by the inverter which switches the available DC-link voltage and provides the desired line-to-line voltage. However, in order to obtain the required value of the line-to-line voltage, it is required to switch the inverter at a modulation index which determines the amount of the peak value of output, fundamental line-to-line voltage. The modulation index is considered as the ratio of the peak line-to-line output

voltage to the DC-link voltage. It can be calculated over the entire speed range for all the values of speed and torque. Now, in order to have a controlled operation of the machine with varying speed and torque, it is required to have a closed-loop control implemented that controls the changes due to the abrupt variations or disturbances occurring in the machine.

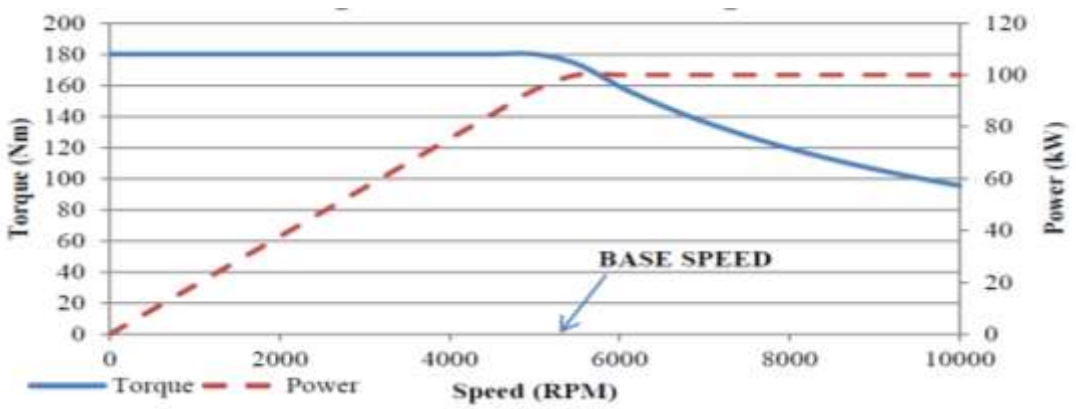

Fig. 3.6 : Torque & Power as a Function of Speed in the Transient Region of Operation

(Source:Spectrum.library.concordia.ca/975146/1/Sejpal_MASc_S2013.pdf)

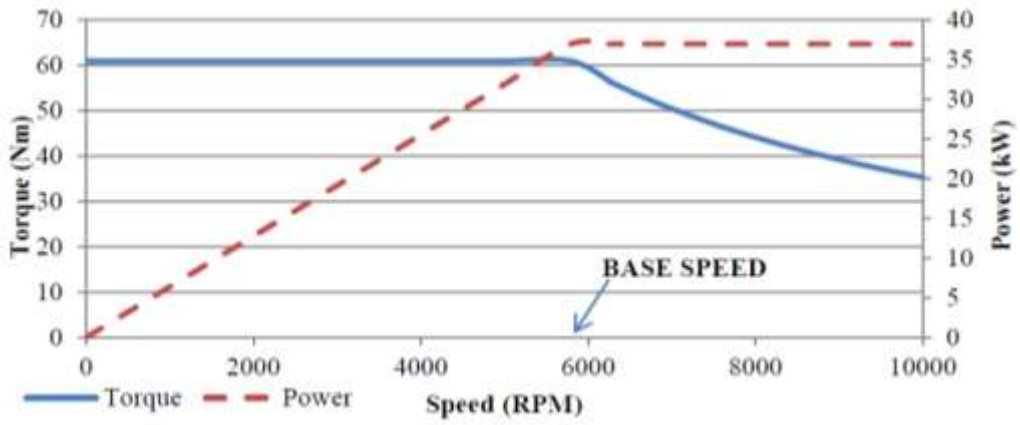

Fig. 3.7 : Torque & Power as a Function of Speed in the Continuous Region of Operation

(source:pectrum.library.concordia.ca/975146/1/Sejpal_MASc_S2013.pdf)

Chapter 4 deals with PMSM drive application in automotive and detail study of multilevel inverter topologies. It also focuses on pulse width modulation(PWM), Space Vector Pulse Width Modulation(SV-PWM) and Carrier-based Space Vector Modulation(CB-SVPWM) Technique.

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CHAPTER – 4

PMSM DRIVE IN AUTOMOTIVE APPLICATION

This chapter focuses on the description of PMSM drive in automotive application. It also discusses the detail study of multilevel inverter topologies and modulation strategies.

4.1 INTRODUCTION

The existing interior Permanent Magnet Synchronous Motor (IPMSM) drive used in Honda Civic 2006 hybrid electrical vehicle shown in fig.4.1.comprised of three parts such as the PMSM motor, the two level voltage source inverter (VSI) and the processor. The motor used in Honda Civic2006 hybrid electrical vehicle is a 3-phase, 15-kW interior PMSM. Its parameters are shown in Table.4.1.

Table 4.1 : The parameters of the tested motor

Pole pairs	**p**	**6**
Stator resistance	Rs	0.0142Ω
d-axis stator inductance	Ld	0.6660mH
q-axis stator inductance	Lq	0.8745mH
Permanent flux	ψf	0.06Wb

(Source: citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.466.6477)

Three single-phase insulated gate bipolar transistor (IGBT) power modules are used in the two level voltage source inverter. SKYPER 32R is used to drive the power module. The cooling style of the inverter is forced water-cooling. The dc link voltage and two-phase stator currents are sensed by isolated devices and fed back to the processor. AD 628 is used to measure the dc-link voltage and LEM HC2F-80s is used to measure stator current. An incremental encoder integrated into the motor is used to determine the rotor position. All the control schemes are implemented on a digital signal processor (DSP) TMS320F2812. The real time software is downloaded from Matlab/Simulink to the DSP directly. The existing PMSM model is as shown in Fig.4.1.It consists of the interior permanent magnet synchronous motor (IPMSM)

motor, a controlled DC motor used to load and a torque meter (Vibro-Meter TG-10BPM3). The current, voltage, torque and speed are the parameters used for simulation purpose. It is seen that,output parameters were observed on LeCroy wave Surfer 44Xs Oscilloscope.

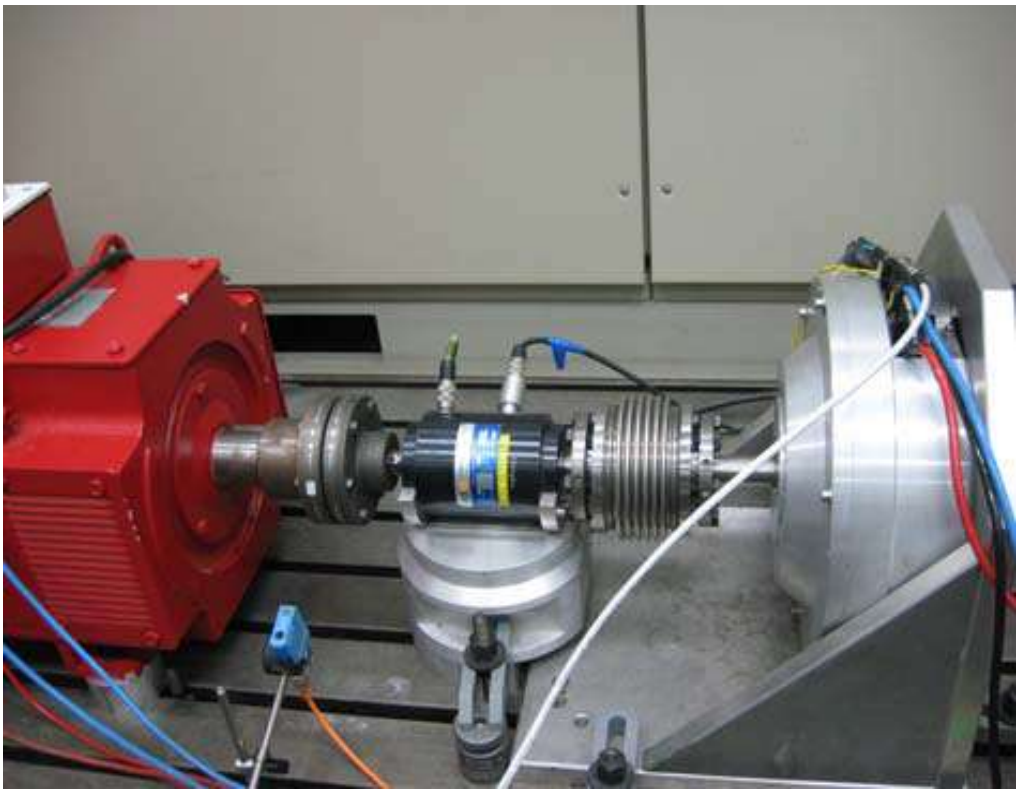

Fig. 4.1 : Honda Civic2006 hybrid electrical vehicle model

(Source: citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.466.6477)

The methology used in existing Honda Civic2006 hybrid electrical vehicle model is namely, the field oriented control (FOC) and the direct torque control (DTC) with voltage selection strategy These two control strategies are compare on the basis of current, voltage, torque and speed. The main drawback of FOC is that it is implemented in the rotor flux reference frame and needs the continuous rotor position information to implement the coordinate transformation and suffer from current and torque ripples and variable switching frequency. Simiarily in DTC, it is implemented in the stationary reference frame and doesn't need the continuous rotor position information except for the initial rotor position. However it controls the current, torque ripples and variable switching frequency up to some extent.

Hence a novel carrier based space vector pulse width modulation (CB-SVPWM) switching technique has been proposed for the DTC in Honda Civic 2006 hybrid electrical vehicle model which can decrease current ripple and fix the switching frequency.

4.2 VOLTAGE SOURCE INVERTER

The 3-φ Voltage Source Inverter (VSI) has to switch the input DC-link voltage and provide the sinusoidal fundamental component of voltage and current to the 3-φ motor, at the output of the inverter. The magnitude and frequency of the sinusoidal output voltage of the inverter controls the speed of the machine that is driven. In the proposed work,at the begining conventional two-level inverter is considered and switched over to multilevel inverter due to drawback of conventional two-level inverter.

4.2.1 Two-Level Inverter

The conventional two-level inverter with a 3-φ PMSM is depicted as shown in Figure 4.2.

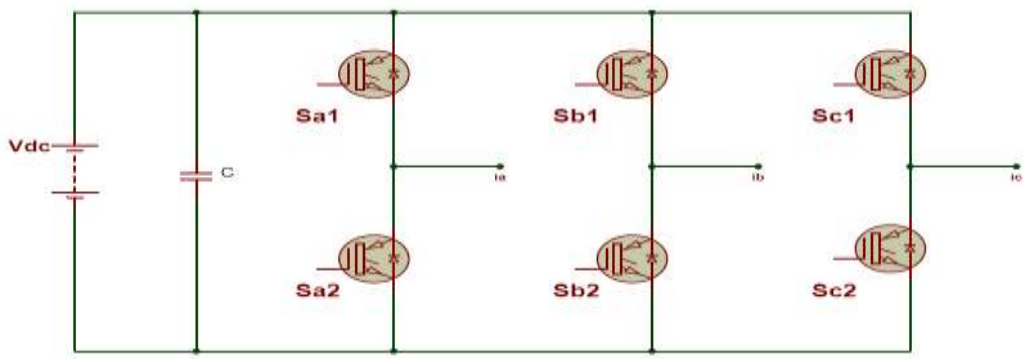

Fig. 4.2 : Conventional, two-level inverter

There are two switches per-phase in a conventional, two-level inverter; and the DC-link capacitor acts as a filter.

Problems associated with conventional adjustable speed drive inverter are as follows.

1. High freqency switching requires significant derating of switching devices and generates large switching losses.
2. High dv/dt because of switching causes motor bearing failure and stator winding insulation breakdown.
3. High frequency switching generates broad band (10 KHz to 30 KHz) Electromagnetic interference (EMI) to near communication.

Multilevel inverters solve these problems because their individual devices have a much lower dv/dt per switching and they operate at high efficiencies because they can switch of a lower frequency than PWM controller inverters.

4.3 INTRODUCTION TO MULTILEVEL INVERTERS

An attempt is made to present the most common multilevel (three-level) inverter and briefly described its advantages and disadvantages based on a literature survey. The literature survey was intended to compare the inverters based on their performance aspects and the challenges and restrictions they could impose for application in the given area. The fundamental purpose of considering multilevel inverters instead of the popular two level inverters is due to the high value of DC-link voltage that needs to be employed in future developments. With increase in DC-link voltage, it is aimed that the performance of the inverter in use does not degrade and hence, multilevel inverter options have been considered. The increase in power-handling capabilities of the power electronic switches has made the use of Voltage Source Inverter (VSI) feasible for high-power applications. For high voltage and high power systems, instead of using switches with high voltage ratings, it is beneficial to connect the switches having low-voltage ratings in series [46]. This would allow the latter to be switched faster than the switches having higher voltage ratings, thus resulting in switching harmonics of higher frequencies which can be filtered out easily. Due to the dynamic voltage sharing problem when the switches are connected in series, multilevel power converters have come into existence and they are being used due to several advantages they offer over the conventional two-level converters. However, in principle, with increased DC-link voltage, there are different ways in which the semiconductor devices can be connected which can be done by series

connection of devices, Dynamic voltage sharing among the devices is a big challenge using switching devices with higher voltage rating but it involves high *dV/dt* stress and renders slower switching due to high voltage level adopting the multilevel solution which is more preferable due to the limited voltage ratings for the semiconductor devices Multilevel converters can be operated at high voltages without the need for series connection of the switching devices. There are different ways in which the devices can be connected so that the dynamic voltage sharing problem posed by the series connection of the devices is no more confronted. The capability of the inverter to operate at high power level with lower harmonic distortion and lower voltage stress across the switches makes it a feasible solution for drives applications. The features that make a multilevel converter an attractive solution, as mention in [47].

4.3.1 Staircase waveform quality

Multilevel inverters can generate output voltage with low distortion and reduced *dV/dt* stresses, resembling a near sinusoidal waveform with increase in the number of levels.

4.3.2 Switching frequency

These inverters can be operated at both fundamental and high switching frequency pulse width modulation (PWM). Lower switching frequency would yield lower switching losses and thus improving the efficiency.

4.3.3 Common-mode voltage

In an inverter-driven A.C. machine, there exists a common-mode voltage as the VSI does not constitute an ideal balanced source. The parasitic capacitances in an A.C. motor become much relevant when this motor is driven by a PWM VSI. High *dV/dt* of the common mode voltage applied across the stator and the ground of the motor (in a 3-φ, 4 wire system) causes pulsed currents (the common-mode currents) to flow through these capacitances thus producing the common-mode voltage. In multilevel inverter-fed motor drive, due to smaller *dV/dt* when compared to the two-level inverter-fed drive, there is smaller common-mode voltage at the motor bearing terminals. There are a number of multilevel converters introduced since the year 1975

but the three basic and most well-known topologies are the Cascaded H-Bridge Multilevel Converter (CHB), Neutral Point-Clamped Multilevel Converter (NPC) and the Flying Capacitor Multilevel Converter (FCC). These three basic topologies have been widely accepted for industrial applications [48]. In order to control the switches of the multilevel inverters, a number of new and modified modulation techniques have been developed [49]. These schemes include the Sinusoidal Pulse Width Modulation (SPWM), Space Vector Modulation (SVM), Selective Harmonic Elimination (SHE), etc. However, in literature, a number of other modified control schemes based on these basic schemes have also been proposed [50].

4.4 BASIC MULTILEVEL INVERTER TOPOLOGIES

A power electronic circuit that could operate in either inverter or rectifier mode is called a converter. Since the present research work concentrates only on the inverter mode of operation of the converter, henceforth, only the term 'inverter' will be used. In the case of a multilevel inverter, the DC-link constitutes more than one capacitor bank as opposed to that in a conventional, two-level inverter which consists of only one capacitor bank. The multiple DC sources formed with the series capacitors are aggregated with the commutation of the power semiconductor switches thus giving a high voltage at the output, and at the same time, each semiconductor switch has to withstand only the reduced level of voltage that appears across each capacitor. The connected DC voltage source determines the rating of the power semiconductor switches. It is difficult to connect a single power semiconductor switch directly to high voltage DC-link, as very high voltage rating of the switch has to be chosen by giving allowance to the voltage overshoot due to the stray inductances present in the semiconductor switch and the module (read as a phase leg of the inverter). The number of levels in a multilevel inverter, in effect, can be defined as the number of levels of phase voltage with respect to the negative terminal of the inverter [51]. Therefore, in case of a two-level inverter, the output voltage with two values (levels) is generated with respect to the negative terminal of the capacitor. A brief introduction about the three basic multilevel (especially, the three-level) inverter topologies has been presented here and depending on the literature survey, the best candidate will be chosen and its detailed comparison will be made with the two-level

inverter for the application in PMSM drive. If 'm' denotes the number of steps (or, levels) of phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between the two phases of the load (or the line voltage at the load side) is denoted by 'k' which is given by

$$k = 2m+1 \tag{4.1}$$

The number of levels in the phase voltage of a three-phase Y-connected load is denoted by 'l' which is given by

$$l = 2k- 1 \tag{4.2}$$

The above relations show that the number of steps of voltage seen by the load is increased in multilevel inverter when compared to the two-level inverter, thus providing a smoother output voltage (nearly sinusoidal) with reduced harmonic distortion. In general, the advantages of utilizing multilevel inverters over the shortcomings of a conventional two-level inverter can be summarized as follows [52]

- The output current of a multilevel inverter has lower distortion when compared to a two-level inverter.
- The multilevel inverter makes better utilization of the DC-bus voltage when compared to the two-level inverter.
- The smaller common-mode voltage of multilevel inverter reduces the stress in the bearings of a motor that is connected to a multilevel motor drive.
- Due to higher number of output voltage levels, the *dV/dt* stress gets reduced which in turn reduces the electromagnetic compatibility (EMC) issues.
- Multilevel inverters can be operated at fundamental as well as low or high switching frequency PWM; high switching frequency renders higher switching losses thus reducing the efficiency of the inverter. There are a few disadvantages of multilevel inverters which can be summarized as follows
- As the number of the required output level increases, the number of the power semiconductor switches required per phase also increases.

Though the voltage rating of the switches required is lower than that of a two-level inverter, each switch demands a related gate drive circuit and this in turn makes the overall system more complex and expensive. Since 1975, plentiful research has been dedicated to multilevel inverter topologies and their modulation schemes. The most promising topologies have been the cascaded H Bridge inverter with separate DC sources, Neutral Point-Clamped or Diode-Clamped inverter and the Flying Capacitors (or Capacitor-Clamped) inverter. The Cascaded H-Bridge multilevel inverter was first introduced in 1975. The idea was to connect the separate DC-sourced full-bridge cells in series so as to synthesize a staircase AC output voltage waveform. Later in 1980s, the diode-clamped multilevel inverter was introduced with diodes blocking the sources. It got its alternate name as neutral-point clamped inverter because the mid-voltage level in three-level inverter was defined as the “neutral” point. The capacitor-clamped multilevel inverter was introduced in the 1990s. They possess a similar structure as that of the diode-clamped multilevel inverter; only that the clamping diodes are replaced by clamping capacitors. The duty of the clamping device is to clamp the voltage level of the switch to that of the DC-link capacitors. Hence, each level in the output staircase waveform represents the voltage of each DC-link capacitor. Therefore, the aggregate of the capacitor voltages gives the output levels (or steps) in the staircase AC waveform. For applications involving high voltage and high power, it is favorable to utilize diode-clamped or capacitor-clamped multilevel inverters to replace the full-bridge cell in a cascaded inverter so as to reduce the number of separate DC sources. Moreover, in applications with limitations in space allowance, and those demanding reduced weight, it is favorable to choose the diode-clamped multilevel inverter as the system would be bulky if capacitors are used for clamping purposes.

4.4.1 Cascaded H-Bridge Multilevel Inverter

In a Cascaded H-Bridge inverter, separate H-bridges are connected in series in each phase depending on the number of levels that are desired at the output. The three-phase structure of a Cascaded H-bridge inverter is shown in Fig.4.3. Separate DC sources are connected to each single-phase full-bridge inverter. The AC output of each level is then connected in series such that the overall output voltage waveform of

the multilevel inverter is the sum of the individual inverter output [53]. From the knowledge of single-phase full-bridge inverters, each inverter level with V_{dc} as the DC voltage for each full-bridge can generate three different voltage outputs; $+V_{dc}$, 0 and $-V_{dc}$ and in case of the inverter represented in Fig.4.3. all the levels from $-2V_{dc}$ to $+2V_{dc}$ are present constituting 5 levels for the phase. This is made possible by connecting the DC sources (or capacitors) sequentially to the AC (output) side via the four power switches present in each cell.

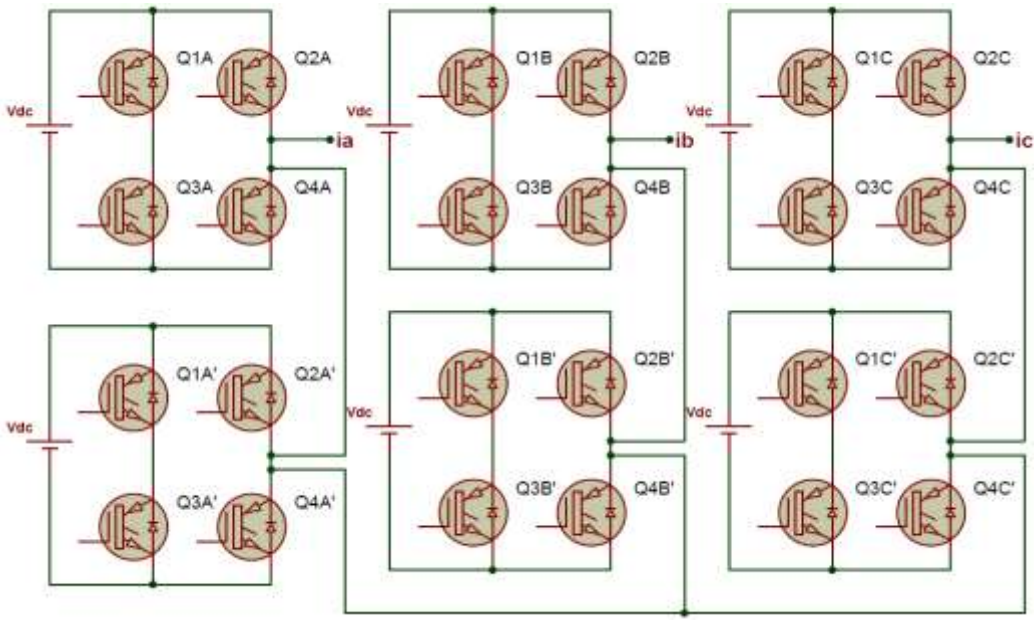

Fig. 4.3 : Three-phase Cascaded H-Bridge Multilevel Inverter

For an m-level cascaded inverter, the number of DC voltage sources‘s’ is related to the number of levels as

$$m = 2s + 1 \tag{4.3}$$

Cascaded inverters have been proposed for use as the main traction drive in electric vehicles where the inverter could serve as a rectifier/charger for the batteries of the vehicle when it is connected to an AC supply. For a vehicle that uses regenerative braking, this inverter can act as a rectifier.

Advantages

- The possible output voltage level is more than twice the number of DC sources.
- Modularity of the series H-bridges make the layout and packaging simple.

Disadvantages

- The main restriction of a cascaded H-bridge inverter is that separate DC sources are required for each of the H-bridges thus limiting its application.
- Separation of batteries or using ultra-capacitors makes the inverter very bulky with higher levels.
- The problem of charge equalization for the separate bridges is an important issue to be taken care of.

4.4.2 Diode Clamped Multilevel Inverter

Since its proposal in 1981, this inverter has found its use in a number of industrial applications. The three-phase structure of a three-level diode-clamped inverter is shown in Fig.4.4.[54]. The three phases of the inverter share a common DC bus. The three-level diode-clamped inverter consists of two series-connected capacitors, C_1 and C_2. The DC-link capacitors divide the DC bus voltage into three levels; namely +Vdc/2,0 & -Vdc/2. These voltage levels appear at the output of each phase of the inverter by appropriate switching of the power semiconductor devices. The middle point of the two capacitors is denoted as 'n' which is the neutral point. There are two complementary switch pairs (S_{a1}, S_{a3}) and (S_{a2}, S_{a4}) and two clamping diodes (D_1, D_{10}) per phase present in this inverter. The outer two switches are the main switching devices (S_{a1}, S_{a4}) that operate for pulse width modulation while the inner two switches are the auxiliary switching devices (S_{a2}, sa_3) that clamp the output terminal potential to the neutral point potential along with the help of the two clamping diodes.

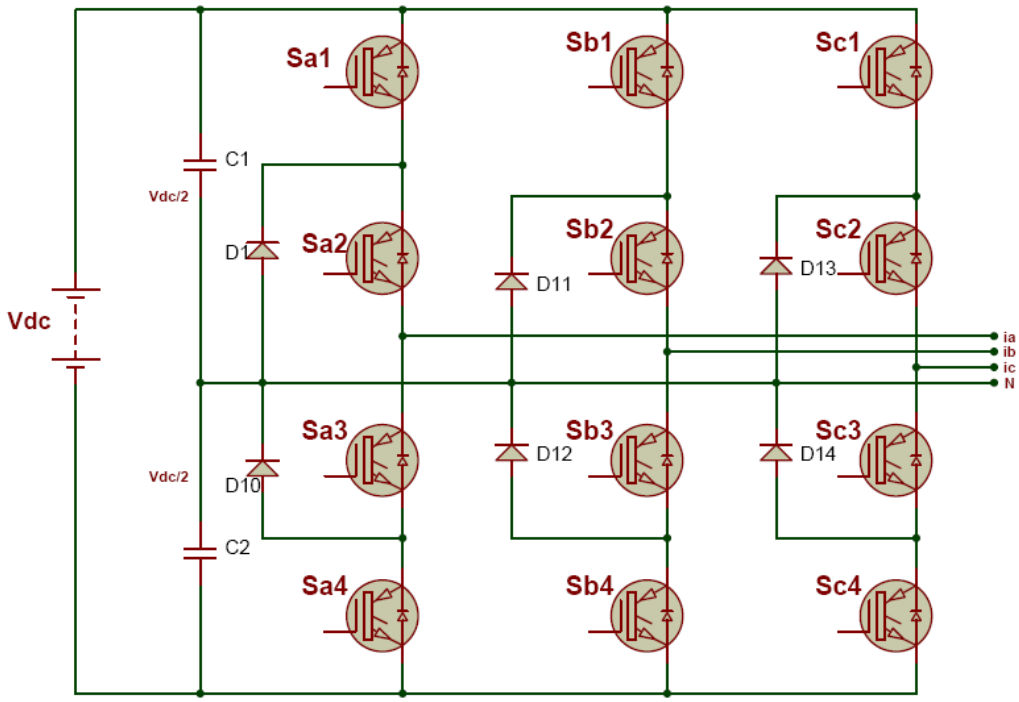

Fig. 4.4 : Three-phase, Three-level Diode-Clamped Inverter

When both the upper switches Sa_1 and Sa_2 turn on, the voltage across 'a' (the first phase) and '0' (the negative inverter terminal), also called the pole voltage, is V_{dc}. The lower clamping diode, D_1, balances out the voltage sharing between the two lower switches, Sa_3 and Sa_4. While the switch Sa_1 **blocks** the voltage across C_1, the switch Sa_2 blocks the voltage across C_2. The voltage between 'a' and '0' is the DC voltage whereas the voltage between 'a' and 'n' is the AC voltage. It is because the voltage appearing with respect to the negative inverter terminal ('0') is the voltage across each capacitor and the voltage appearing with respect to the neutral point of the inverter ('n') is the aggregate of the capacitor voltages; giving an AC waveform. In order to obtain three levels across 'a' and 'n', there are three switch combinations as follows:

Turn on upper switches, Sa_1 and Sa_2, in order to obtain V_{an} =+Vdc/2.

Turn on middle switches, Sa_2 and Sa_3 in order to obtain V_{an} = 0.

Turn on lower switches, S_{a3} **and** S_{a4} in order to obtain V_{an} =-Vdc/2

Advantages

- The three phases share a common DC-bus minimizing the capacitance requirements.
- The DC-link capacitors can be pre-charged, as a group.
- High efficiency for fundamental frequency switching.

Disadvantages

- Increased number of clamping diodes.
- Neutral point control for balanced voltages across the DC-link capacitors should be achieved for all conditions of operation.

4.4.3 Flying Capacitor Multilevel Inverter

The Flying Capacitor multilevel inverter came into existence in 1992. The three phases of three-level Flying Capacitor inverter is shown in Fig.4.5. The three phases of the inverter share a common DC bus. Similar to the three-level Diode-Clamped multilevel inverter, the Capacitor-Clamped multilevel inverter has two series-connected capacitors, C_1 and C_2, dividing the DC bus voltage into three levels; namely +Vdc/2,0,-Vdc/2. .

These voltage levels appear at the output of each phase of the inverter by appropriate switching of the power semiconductor devices. In place of the “clamping diodes” present in the diode-clamped multilevel inverter, the capacitor-clamped multilevel inverter consists of “clamping capacitors”. Each clamping capacitor clamps the device voltage to one DC-link capacitor voltage level [55].

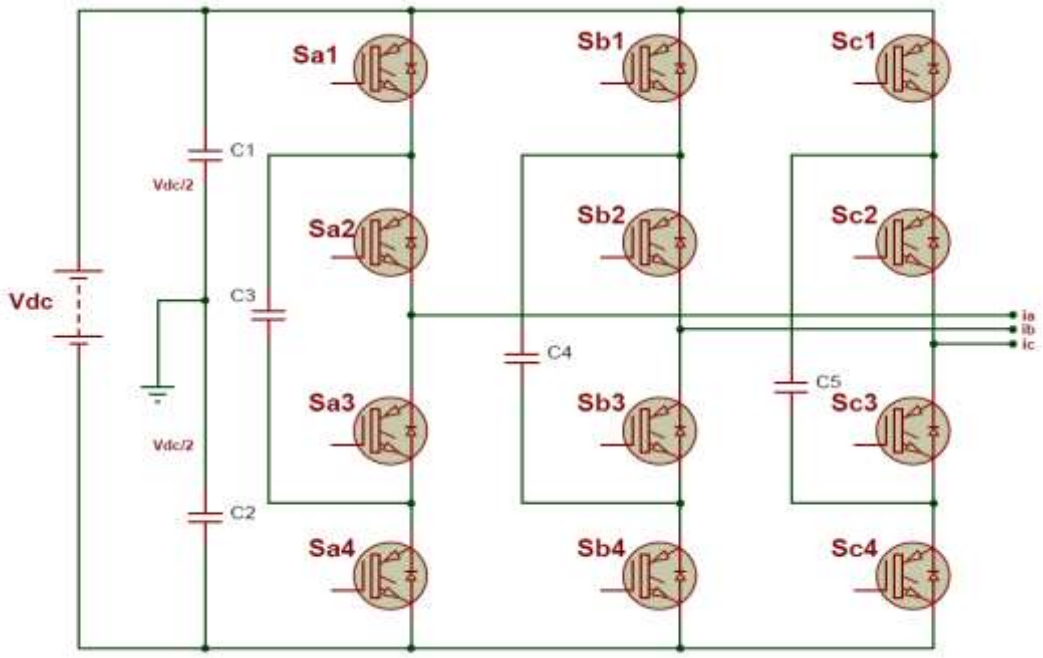

Fig. 4.5 : Three-phase Capacitor-Clamped Multilevel Inverter

In order to obtain three levels across 'a' and 'n', there are three switch combinations as follows: Turn on upper switches, Sa_1 and Sa_2, in order to obtain V_{an} =+Vdc/2

Turn on switches, (Sa_1, Sa3) or (Sa_2, S_{a4}), in order to obtain V_{an} = 0.

Turn on lower switches, Sa_3 **and** Sa_4 in order to obtain V_{an} =-Vdc/2

During the zero output voltage, the clamping capacitor C_3 is charged when the switch pair (Sa_1 , Sa_3) is turned on; and C_3 is discharged when the switch pair (Sa_2, Sa_4) is turned on.

Advantages

- Availability of switching redundancy for capacitor voltage balance.
- Increased number of capacitors allows the inverter to ride through short duration outages.

Disadvantages

- Increased number of capacitors makes the system very bulky with increased losses.

- capacitor voltage levels have to be maintained at all times.
- The capacitors require a separate pre-charge circuit.
- Cost increases manifold due to the increased number of capacitors in the capacitor- clamped topology when compared to the clamping diodes in the diode-clamped topology.

4.5. MODULATION TECHNIQUES

4.5.1 Pulse Width Modulation

The basic control method in power electronics is the Pulse-width modulation (PWM). Except some resonant converters, majority of power electronic circuits are controlled by PWM signals of various forms. In this technique the duty ratio of a pulsating wave-form is controlled by another input waveform. The ON and OFF times of the switches can be obtained by the intersections between the reference voltage waveform and the carrier waveform. By changing the duty ratio of the switches the speed of the motor can be changed. The longer the pulse is closed higher the power supplied to the load. The change of state between closing (ON) and opening (OFF) is rapid, so that the average power dissipation is very low compared to the power being delivered. The theoretically zero rise and fall time of an ideal PWM waveform represents a preferred way of driving modern semiconductor power devices The rapid rising and falling edges ensure that the semiconductor power devices are turned on or turned off as fast as practically possible to minimize the switching transition time and the associated switching losses.

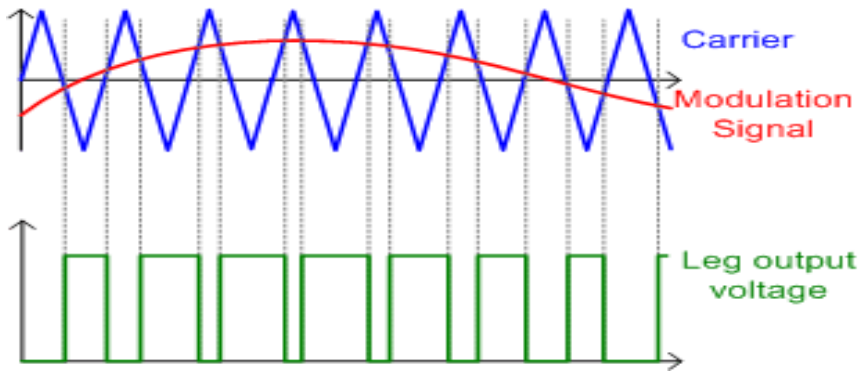

Fig. 4.6 : Pulse width modulation

4.5.2 Space Vector Pulse Width Modulation

The conventional DTC system of permanent magnet synchronous motor has a simple control structure and fine static and dynamic performance. However, in the conventional DTC system, the switchover among the basic vectors is discontinuous because the universal voltage inverter has only eight available basic space vectors, while 6 of them are nonzero and distribute in space every 60 degree. In a control period, only one voltage space vector can be selected, which could not adjust the direction and control the range ability of stator flux. So flux and torque ripple is unavoidable.

In a control period, two adjacent nonzero voltage vectors and zero vectors are selected and their action time is calculated in order to synthesize the voltage space vector needed and then control the inverter. This method abandons that this method can reduce the torque and flux ripple caused by hysteretic controller efficiently.

4.5.3 Carrier Based Space Vector Pulse Width Modulation

In the conventional Sinusoidal Pulse Width Modulation (SPWM) strategy, the amplitude modulation index controls the fundamental frequency component of the output voltage. However, in this case, the maximum value of the fundamental component of the line-to line output voltage is only 61.2% of the DC-link voltage, at the maximum modulation index in the linear range of 1. This presents a poor utilization of the voltage available at the DC-link. In order to make better utilization of the DC-link voltage, one needs to go beyond the linear range of the modulation index, which is the over-modulation range, thus boosting the fundamental frequency component of the output voltage to 74.4% for square-wave operation. However, in the over-modulation range, the amplitude modulation index has a non-linear relationship with the fundamental line-to-line output voltage as opposed to the linear range where the two quantities share a linear relationship. Though the output voltage can be increased by employing over-modulation, it also introduces low-order harmonic components which are difficult to filter by the load inductance. To fulfill a similar objective of boosting the fundamental component of output voltage, another approach can be followed which does not introduce any lower order harmonics. This approach is the Carrier-based Space Vector Modulation, which in simple terms means the

realization of Space Vector Modulation using the conventional Carrier-based approach. The approach for using Carrier-based Space Vector Modulation (CB-SVM) for three-level inverters will be discussed in the upcoming sections.

In case of a three-level inverter, as there are four switches per phase of the inverter, two triangular carriers are therefore required so that the four switches could be turned-on and –off complementarily. It is now required to know as to how to place the two triangular carriers so that the harmonic content is not high. However, from literature, it is known that the Phase Disposition (PD) PWM method is the most preferable due to lower Total Harmonic Distortion (THD) in the output waveform.

i) Basic Properties

A carrier-based PWM modulator is comprised of modulation signals and carrier signal. The operation of PWM can be divided into two modes.

1) *Linear Mode.*—In the linear mode, the peak of a modulation signal is less than or equal to the peak of the carrier

   Signal. When the carrier frequency is greater than 20 modulation signal frequency, the gain of PWM G ~ 1

2) *Nonlinear Mode*—When the peak of a modulation signal is greater than the peak of the carrier signal, over modulation occurs with G < 1. The six-step mode marks the end of the nonlinear mode. The THD of output switched Waveforms increases.

ii) Carrier-Based PWM

A universal representation of modulation signals for three-phase carrier PWM modulators is as follows

$$u_i(t) = u_i^*(t) + e_i(t) \qquad (4.4)$$

Where e_i (t) are injected harmonics, and u_i^* are called fundamental signals that are three-phase symmetrical sinusoidal signals as follows.

$$u_a^*(t) = m \sin \omega t$$

$$u_b^*(t) = m \sin(\omega t + 2\pi/3)$$

$$u_c^*(t) = m \sin(\omega t + 4\pi/3) \qquad (4.5)$$

Where is m the modulation index, and $u_a^*(t) + u_b^*(t) + u_c^*(t) = 0$

The output line-to-neutral voltages are

$UaN(t) = [E/2]\,[m \sin \omega t + e_i(t)]$

$UbN(t) = [E/2]\,[m \sin(\omega t + 2\pi/3) + e_i(t)]$

$UcN(t) = [E/2]\,[m \sin(\omega t + 4\pi/3) + e_i(t)]$ (4.6)

The output line-to-line voltages Uab, Ubc, and Uca are

$Uab(t) = UaN(t) - UbN(t)$

$= [E/2]\,[m \sin(\omega t + \pi/6)$

$Ubc(t) = [E/2]\,[\sqrt{3} m \sin(\omega t + 5\pi/6)$

$Uca(t) = [E/2]\,[\sqrt{3} m \sin(\omega t + 3\pi/6)$ (4.7)

In the linear modulation range, (15) , (16), and $|u_i| \leq 1$ show that output line-to-line voltages are equal to or less than dc-bus voltage E. Therefore, the possible maximum modulation index m_{max} is $2/\sqrt{3}$ in the linear range.

It is clear that the injected harmonics do not appear in the line to line voltages.

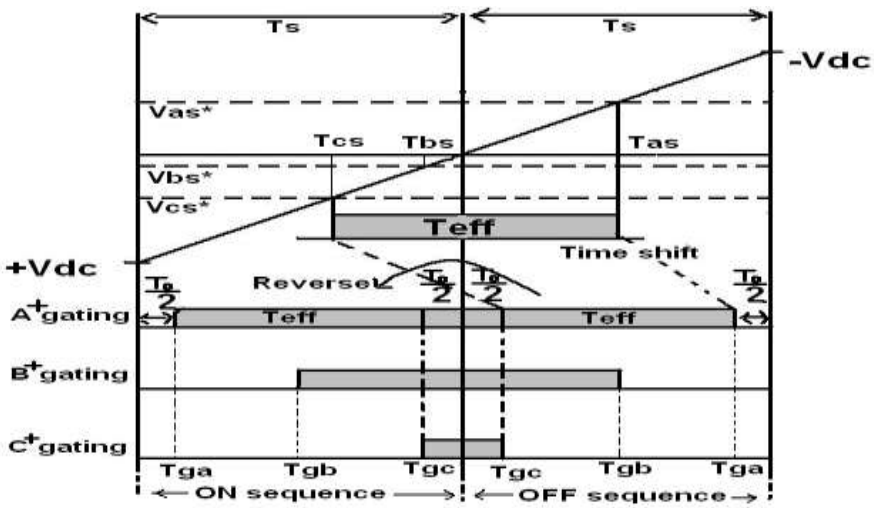

Fig. 4.7 : Actual gating time generation for CBSVPWM

The main requirements for high performance PWM inverter-fed PMSM drive can be formulated as follows:

- Fast flux and torque response
- Available maximum output torque in wide range of speed operation region
- Constant switching frequency
- Uni-polar voltage PWM
- Low flux and torque ripples
- Robustness to parameters variation
- Four quadrant operation

4.6 CONCLUSION

It has been seen from the results of detailed comparisons made by the various researchers all around the world, the diode-clamped inverter topology stands out as the best inverter of choice for the automotive applications in drives providing better Total harmonic distortion(THD)spectrum and lower losses than the conventional two-level inverter. Therefore, in present research work the three-level diode clamped inverter topologies is proposed.

Chapter 5 deals with control strategy used for permanent magnet motor control, A Scalar control &vector control techniques are also explained in detail.

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CHAPTER- 5

CONTROL STRATEGY OF PERMANENT MAGNET SYNCHRONOUS MOTOR DRIVE

This Chapter focuses on control strategy of Permanent Magnet Synchronous Motor drive. A Scalar and vector control techniques are explain in details and also different types of vector control methods have been elaborated.

5.1 INTRODUCTION

PMSM control techniques are classified as scalar and vector control. Scalar control is based on relationships valid in steady-state. Frequency and amplitude of the controlled variables are being considered. In vector control amplitude and position of a controlled space vector is considered. Above relationships are true even during transients who are essential for precise torque and speed control.

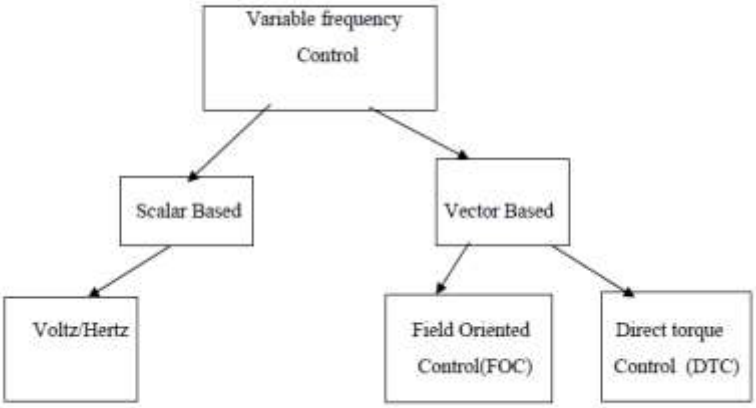

Fig. 5.1 : Some Common Control Techniques Used For PMSM

5.2 SCALAR CONTROL

Scalar control is based on relationships considered to be true in steady state.It is to be worth noted that only magnitude and frequency of voltage, current, etc. are controlled. Scalar control is used where several motors are driven in parallel by the same inverter. Volts/Hertz control is such a simple control scheme for motor control. The control is an open-loop scheme and does not use any feedback loops.

5.3 VECTOR CONTROL

The problem with scalar control is that motor flux as well as motor torque in general are coupled which affects the response and makes the system prone to instability if it is not considered. However in the vector control, the magnitude of the stator and rotor flux along with their mutual angle is considered.

In order meet the above requirements, various control methods have been proposed and implemented [56,57,58].

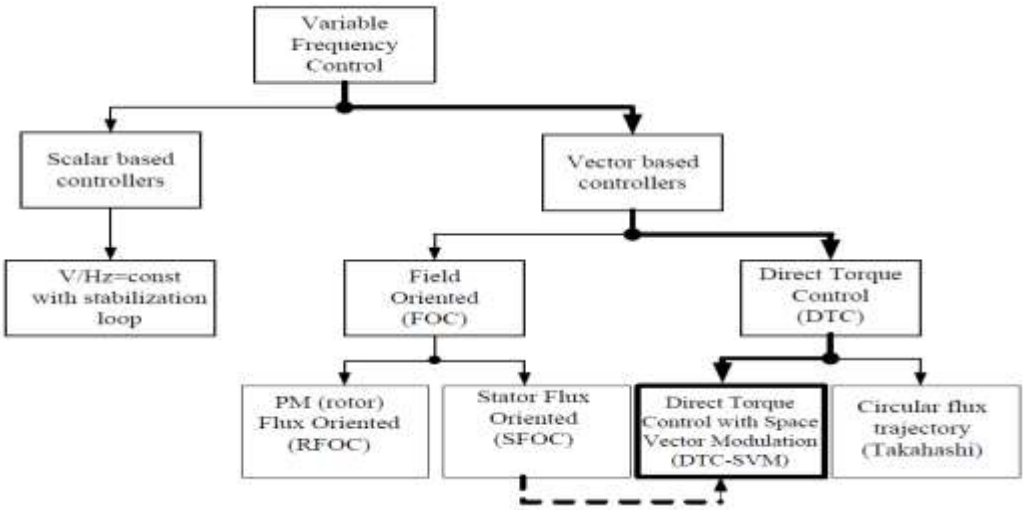

Fig. 5.2 : Classification of PMSM control methods

The general classification of the variable frequency control for PMSM is presented in Fig. 5.2.

5.4. PRINCIPLE OF FIELD ORIENTED CONTROL (FOC)

Field Oriented Control which was invented in the beginning of 1970's usually refers to controllers which maintain a 90° electrical between rotor and stator field components. Systems which depart from the 90° orientation are referred to as field angle control. Vector control is actually control of phase and amplitude of the motor stator voltage/current vector at the same time. The motor torque is dependent upon the stator current which has the components *id* and *iq*. It is possible to control motor torque by *id* and *iq*. Current id is for excitation. $id = 0$ is set for the control strategy. Torque can be obtained only by the q axis current *iq*. So let $id = 0$, through control the

iq, we are achieving Maximum torque control in the PMSM vector control can be achieved by controlling *iq* and *id = 0.*

The principle of the FOC is based on an analogy to the separate excited d.c motor. FOC of PMSM is an important variation of vector control methods. The objective of the FOC method is to control the magnetic field and electromagnetic torque by controlling the d and q axes components of the stator currents. With the information of the stator reference currents and the rotor angle a FOC method can control the motor torque and the flux effectively. The main advantages of this method are the fast response and the less torque ripple. The implementation of this method will be carried by implementing two current regulators, one for the direct-axis component, quadrature-axis component and one speed regulator. The block diagram of the FOC method is shown in fig.1.3, Chapter-1.

To maintain the amplitude of the rotor flux linkage Ψ_r at a fixed value is the main objective of FOC, except for field weakening operation and only to modify a torque-producing quadrature component for controlling the torque of the alternating machine. This control method is based on projections. By the interaction of stator flux linkages and stator currents producing the electromagnetic torque which can be expressed as a complex product of the flux and current space phasors. In order to completely decouple torque and the flux, the current phasor i_s is transformed into two components of a rotating reference frame: A flux producing component i_d aligned with direct axis representing the direction of the rotor flux, also a torque producing component i_q aligned with the quadrature axis perpendicular to the rotor axis. Thus the electromagnetic torque can be controlled by the quadrature -axis current itself. This is equivalent to the torque control of a separately excited dc machine.

5.4.1 Field Oriented Control (FOC) of PMSM

The goal of the FOC is to control the d and q-axis current i_d and i_q to achieve required torque. By controlling *id* and *iq* independently we get a maximum torque per Ampere ratio to minimize the current needed for a specific torque, which increases the motor efficiency. In case of a non-salient machine, control technique can be easily

implemented because *Ld=Lq* and produces only one torque i.e electromechanical torque,

$$T_e = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\left(\lambda_{pm} i_{qs}\right) \tag{5.1}$$

From the above equation (1) the torque producing current will be along the q-axis. To reach maximum efficiency, the torque per ampere relationship should be maximum. This can be easily obtained by keeping i_d =0 at all times.

For salient pole machine the direct and quadrature axis inductances are unequal and also for the actual steady state operation the torque equation is given as:

$$T_e = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\left(\lambda_{pm} i_{qs} - (L_q - L_d) i_{qs} i_{ds}\right) \tag{5.2}$$

From the above eq.5.2. there are two terms affecting in equations (5.3) and (5.4) the torque production, the electromechanical torque and the reluctance torque is

$$T_e = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\left(\lambda_{pm} i_{qs}\right) \tag{5.3}$$

(5.3))

$$T_r = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\left((L_q - L_d) i_{qs} i_{ds}\right) \tag{5.4}$$

5.4.2 Closed loop PI control using FOC of PMSM

The block diagram of closed loop PI control using FOC to investigate the speed and torque control with different modulation techniques such as pulse width modulation, space vector pulse width modulation and carrier based space vector pulse width modulation for a voltage source three-level diode clamped inverter fed PMSM is presented in fig.1.3,chapter-1.

Every time the currents and the voltages are measured and transformed into a-β reference frame. The currents are further converted into *d-q* frame using Park Transformation. The reference speed being compared with the motor speed will give the error which is given to the PI controller. The PI controller output will be taken as

q axis current *iq*. The reference direct-axis current *id* =0 is considered. The reference direct-axis current will be compared with transformed current and its output is given to another PI controller.

The Output of PI controllers goes to current controller .This will generate voltages *Vd* and *Vq*. From these voltages, reference voltages can be generated using different modulation techniques. The Switch is used to carry out three modulation techniques. The reference waves which are generated compared with the triangular waves and the pulses are obtained which are given to the 12 IGBT's of the three level diode clamped inverter. The output of the inverter is given to the PMSM to control the speed and torque of the motor.

5.5 PRINCIPLE OF CONVENTIONAL DTC

The Direct Torque Control (DTC) which was introduced in the 1980's particularly for Induction Machines for flux and torque control was later developed for PMSMs in late 1990's. The DTC is gaining excessive popularity because of its simple control structure and easiest implementation.

The principle of DTC is to directly select voltage vectors according to the differences between the reference and the actual values of torques and flux linkages. The actual values of torque and flux errors are compared by using hysteresis comparators and voltage vector is selected accordingly from a table. Advantages of the direct torque control are simplicity and that it only need to use of one motor parameter, the stator resistance. However no PWM is needed; instead of it one of the six VSI voltage vectors has to be applied during the complete sample period. All calculations are performed in a stationary reference frame which does not involve the actual knowledge regarding the rotor position. The DTC hence require very low computational power when applied digitally. The system have good dynamic performance but it shows quite poor performance during the steady-state since the crude voltage selection criteria give rise to higher ripple levels in flux linkage, stator current, and torque. For every doubling in sample frequency, the ripple will approximately halved.

The basic principle in conventional DTC for PMSM is to directly select stator voltage vectors by means of a hysteresis stator flux and torque control. The stator flux Ψ_s^* and torque T_e^* are compared with the corresponding estimated values of both stator flux as well as torque errors are processed by means of hysteresis band comparators. In particular, stator flux is being controlled using a two level hysteresis comparator, whereas the torque is being controlled using a three level comparator. On the basis of the hysteresis comparators and stator flux sector a VSI voltage vector will be selected using the switching table.

5.5.1 DTC of PMSM

The basic principle of Direct Torque Control (DTC) is to estimate the torque and flux errors from hysteresis comparators and to directly select voltage vectors based on the differences between reference and actual value of torque and also the flux linkage. Advantages of DTC are low complexity, low computational power, and good dynamic performance. The basic concept is controlling the stator flux vector in amplitude and angular position. Let λ_s be the stator flux linkage vector and λ_r be the rotor flux linkage vector in d-q coordinate.

The PMSM stator flux linkage and torque equations in the d-q coordinate system are follows:

$$\lambda_D = L_D I_D + \lambda_R \tag{5.5}$$

$$\lambda_Q = L_Q I_Q \tag{5.6}$$

$$\lambda_s = \sqrt{(\lambda_D^2 + \lambda_Q^2)} \tag{5.7}$$

$$T_{EM} = \left(\frac{3}{2}\right) P\left(\lambda_D I_Q - \lambda_Q I_D\right) \tag{5.8}$$

Where p=pole pairs of the motor.

Now, the d-q current and flux linkage equation can be written as

$$I_D = \frac{\lambda_D - \lambda_Q}{L_D} \tag{5.9}$$

$$I_D = \frac{\lambda_D}{L_Q} \tag{5.10}$$

$$\lambda_D = \lambda_S \cos\delta \tag{5.11}$$

$$\lambda_Q = \lambda_S \sin\delta \tag{5.12}$$

Substituting the above equations in the torque expression

$$T_{EM} = \left(\frac{3}{2}\right) P \frac{|\lambda_S|}{2L_D L_Q} \left(2\lambda_R L_Q \sin\delta - |\lambda_S|(L_Q - L_D)\sin 2\delta\right) \tag{5.13}$$

The main disadvantage of conventional DTC is high ripple levels in stator current, flux linkage and torque, due to the application of same active voltage vector during the whole sample period and possibly several consecutive sample intervals. This can be overcome by using proper modulation technique which is a Space Vector Modulation (SVM) which synthesizes any voltage vector lying inside the sextant. In DTC-SVM the hysteresis comparators are replaced by an estimator which calculates an appropriate voltage vector to compensate for torque and flux errors. It gives good dynamic performance with less torque and flux ripple but is more complex and lose an essential feature of DTC, its simplicity. To reduce the complexity involved in SVPWM, a novel modulation technique named Unified voltage modulation or carrier based space vector pulse width modulation (CBSVPWM) is described using the concept of effective time. By using this method the inverter output voltage which is being directly synthesized by the effective times and the voltage modulation task can be greatly simplified. The actual gating signals for each inverter arm can be easily deduced as a simple form using the effective time relocation algorithm. The block diagram of the DTC-CBSVPWM fed SPMSM using three-level diode clamped inverter is shown in fig.1.4, chapter-1. The measured currents from the motor are transformed to *α-β* by using Clarke transformation. The voltage is estimated from the inverter switching state and the DC-link voltage in the α-β reference frame.

The block diagram of the DTC-CBSVM fed PMSM using three level diode clamped inverter is shown in fig.1.4, chapter-1. The measured currents from the motor are transformed to *α-β* by using Clarke transformation. The voltage is estimated from

the inverter switching state and the DC-link voltage in the α-β reference frame. Now stator flux is estimated as

$$\phi_{\alpha\beta} = \int (V_{\alpha\beta} - R_S I_{\alpha\beta})dt \tag{5.5}$$

The magnitude of this estimated flux is compared with the required flux ϕs*. Then the torque is estimated as,

$$T_E = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\left(\lambda_{S\alpha} I_{S\beta} - \lambda_{S\beta} I_{S\alpha}\right) \tag{5.6}$$

and is compared with the required torque *T** after which the flux and torque errors go to flux-hysteresis and torque hysteresis comparators respectively. The output of the comparators is given to CBSPWM from which the reference wave is generated similar to SVPWM. This reference wave will be compared with the triangular waves same in case as PWM. The number of carrier waves required for three-level inverter is 2. From this the pulses are generated for the three-level diode clamped inverter which have 12 IGBT's. The inverter output goes to the surface-mounted PMSM drive whose speed and torque are to be controlled.[59]

Chapter 6 deals with Simulation model & results of PMSM drive of FOC and DTC based three level diode clamped multilevel inverter fed PMSM drive under Steady state and transient state condition.

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CHAPTER – 6
SIMULATION MODEL AND RESULTS OF PMSM DRIVE

This Chapter deals with simulation models and results of FOC & DTC based multilevel inverter fed PMSM drive under steady state & transient condition for different modulation techaniques.MATLAB/ Simulink® 2014a version software is used to perform the simulation during this research work. Different models have been developed for different speed control scheme in accordance with the theoretical aspects discussed in chapter 5 All the simulations are performed in discrete environment with sampling time in the order of microseconds.

6.1 INTRODUCTION

Field oriented control and Direct torque control of PMSM drive using carrier based space vector modulation scheme with a 3-level diode clamped inverter has been evaluated based on the simulation done in Matlab/Simulink®2014b. A PMSM which has the parameters

Ld=0.006365H;Lq=0.006365H;R=1.6Ω;PM_flux=0.1852Wb;P=2;
F=0.00005396 Nm-s; J=0.0001854 Kgm^2 has been selected for simulation.

The dc link voltage is kept at 380V, the sampling time chosen is Ts=0.0004sec (fs=2.5 kHz) and the applied value of load torque is 3Nm. The motor is started from standstill with an applied load of 3Nm to a reference speed of 1200 rpm. The PI speed controller comes into action and track the reference speed. And motor develops a torque equal to the load torque.

The simulation of the PMSM electrical drive two levels & three level diode clamped IGBT inverter system is investigated. The control scheme applied for the electrical drive is the field oriented control (F.O.C) and direct torque control(DTC) using carrier based pulse width modulation (CBSVPWM) techniques have been applied to the field oriented control (F.O.C) and direct torque control(DTC) based

three level diode clamped inverter. The system used was investigated for steady and transient state. The models was implemented and simulated for Permanent Magnet Synchronous Motor in the Matlab-Simulink environment. The load torque applied is step. Fig.6.1, Fig.6.3 and Fig.6.5.shows simulation models of FOC and DTC based two-level inverter and Matrix Converter fed PMSM drive using SVPWM. Fig.6.2, Fig.6.4 and Fig.6.6 .shows output response of FOC and DTC based two-level inverter and Matrix Converter fed PMSM drive using SVPWM and Fig.6.7 .FFT analysis of DTC with Matrix Converter.

Fig.6.8 & Fig.6.10 shows simulation model of three levels diode clamped inverter fed PMSM drive using PWM SVM. Fig.6.12 (a) & Fig. 6.12(b) shows inverter line voltage waveform using FOC- PWM & FOC- SV-PWM. Fig.6.13 (a) & Fig.6.13(b) shows inverter phase voltage waveform using FOC- PWM & FOC- SV-PWM. Fig. 6.14 (a) & Fig.6.14(b) shows single phase line voltage waveform using FOC- PWM & FOC- SV-PWM. Fig.6.15 (a) & Fig.6.15(b) shows single phase phase voltage waveform using FOC- PWM & FOC- SV-PWM. Fig.6.16 (a) & Fig.6.16(b) shows three phase current waveform using FOC- PWM&FOC- SV-PWM. Fig.6.17 (a) & Fig.6.17(b) shows single phase current waveform using FOC- PWM & FOC-SV-PWM. Fig. 6.18 (a) & 6.18 (b) shows the Output speed response using FOC-PWM & FOC- SV-PWM. Fig.6.19 (a) & 6.19(b) shows the Output torque response using FOC- PWM & FOC- SV-PWM. Fig.6.20 (a) & 6.20 (b) shows the Output stator current response using FOC-PWM & FOC- SV-PWM. Fig.6.21 (a) & 6.21 (b) shows the motor voltage response using FOC- PWM&FOC- SV-PWM. Fig.6.22. shows simulation model of three level diode clamped inverter fed PMSM drive using FOC-CBSVM. Fig. 6.24. shows output waveforms of CB-SVPWM inverter. Fig.6.25. Shows simulation model of three level diode clamped inverter fed PMSM drive with DTC-CBSVM.

6.2 SIMULATION MODELS OF TWO LEVEL INVERTER FED PMSM DRIVE

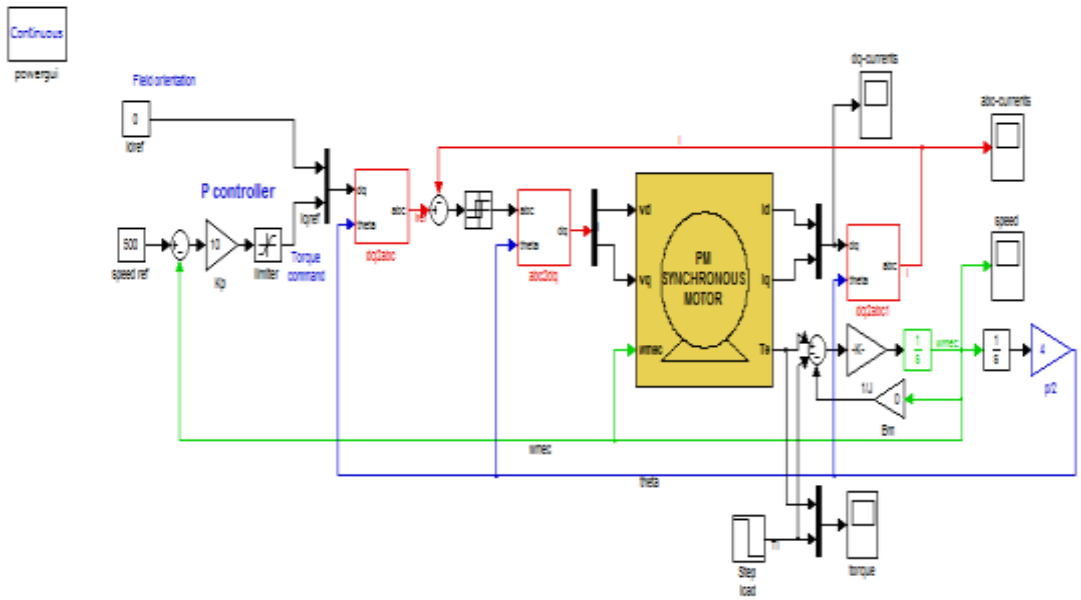


Fig. 6.1 : Simulink model of FOC

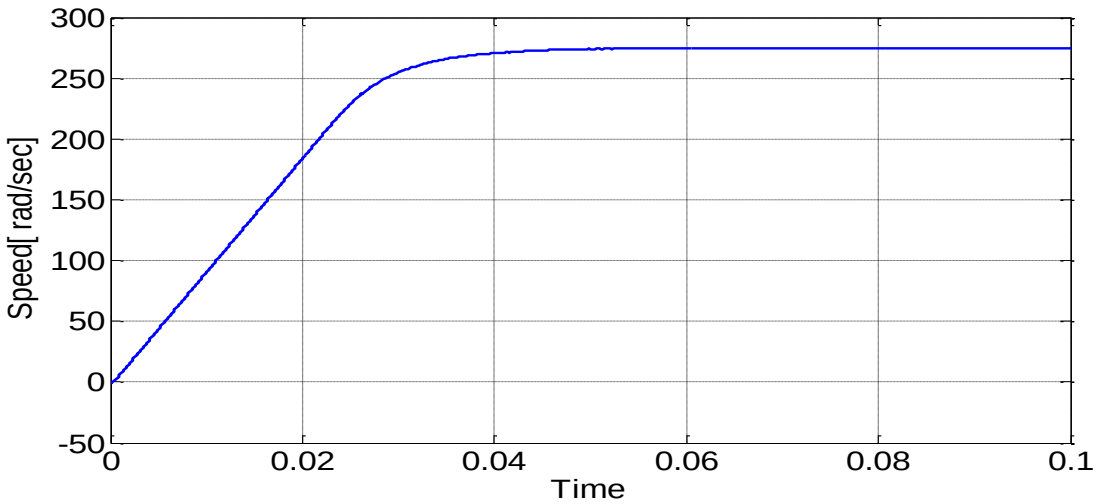


Fig. 6.2 (a) : Speed response using FOC- SVM

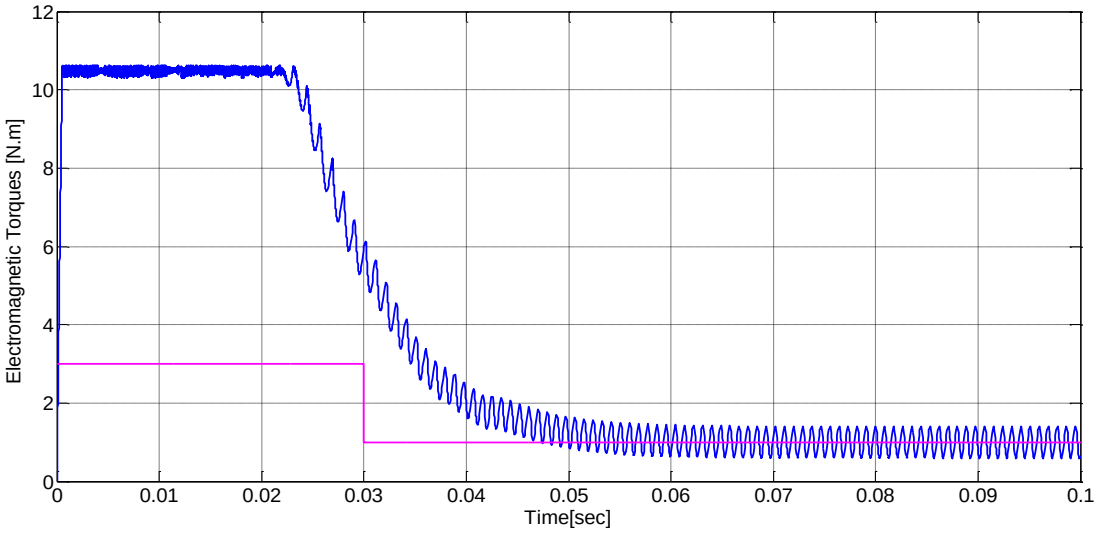


Fig.6.2 (b) : Electromagnetic torque response using FOC- SVM

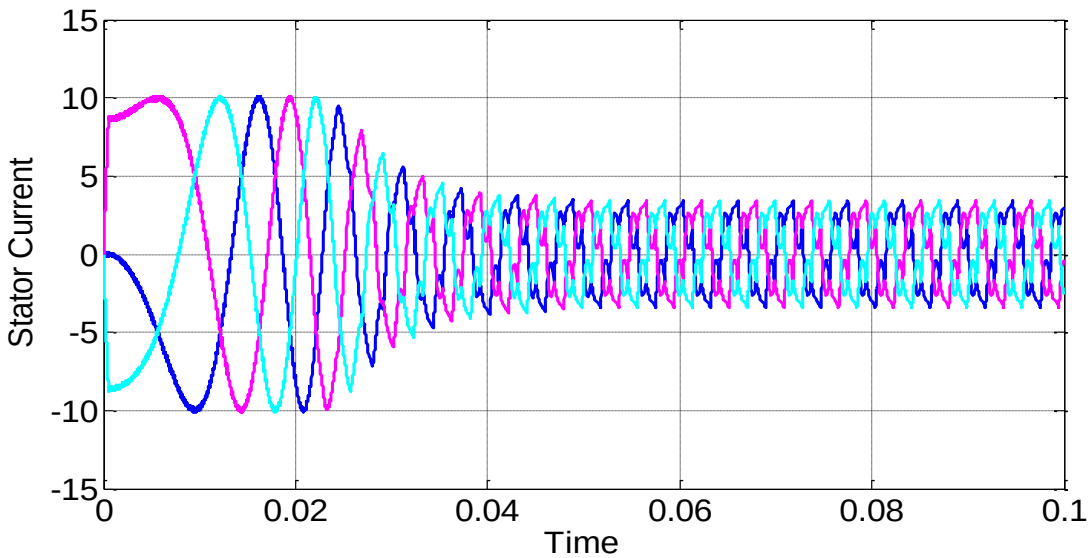


Fig.6.2(c) : Three phase stator current response using FOC- SVM

In Fig.6.2 (b) load torque of 3 N-m is applied at 0.01s of the simulation and removed in 0.03 sec .The electromagnetic torque varies in accordance with the load torque. the reference speed is 500 rpm and there is fluctuation in speed at instant of application or removal of torque though speed practically remains constant. At 0.06s speed, three phase stator current &electromagnetic torque is constant with some ripples.

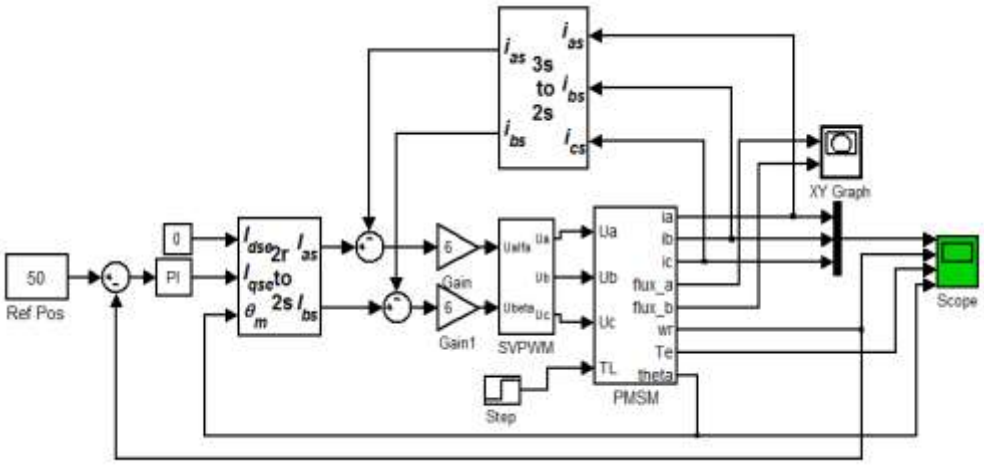


Fig. 6.3 : Simulink model of SVM-DTC

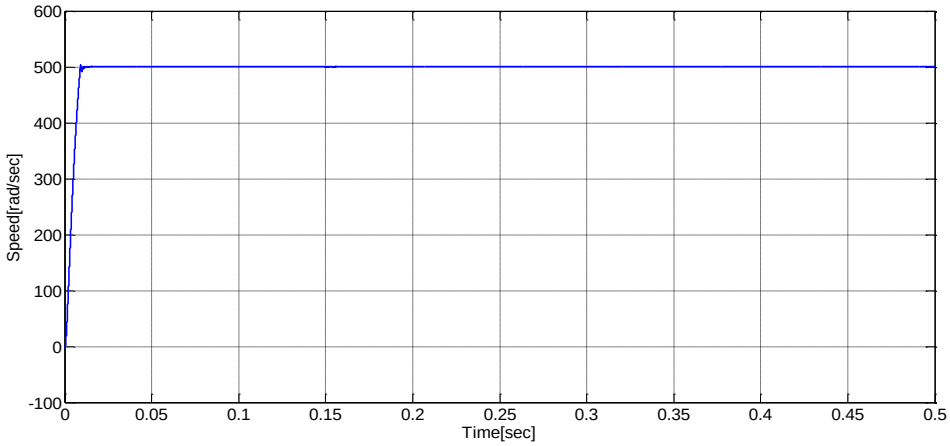


Fig. 6.4(a) : Speed response using DTC- SVM

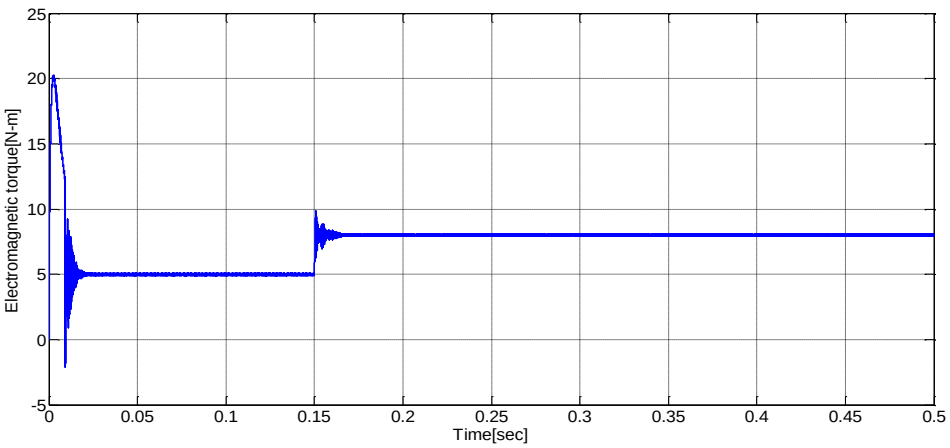


Fig.6.4 (b) : Electromagnetic torque response using DTC- SVM

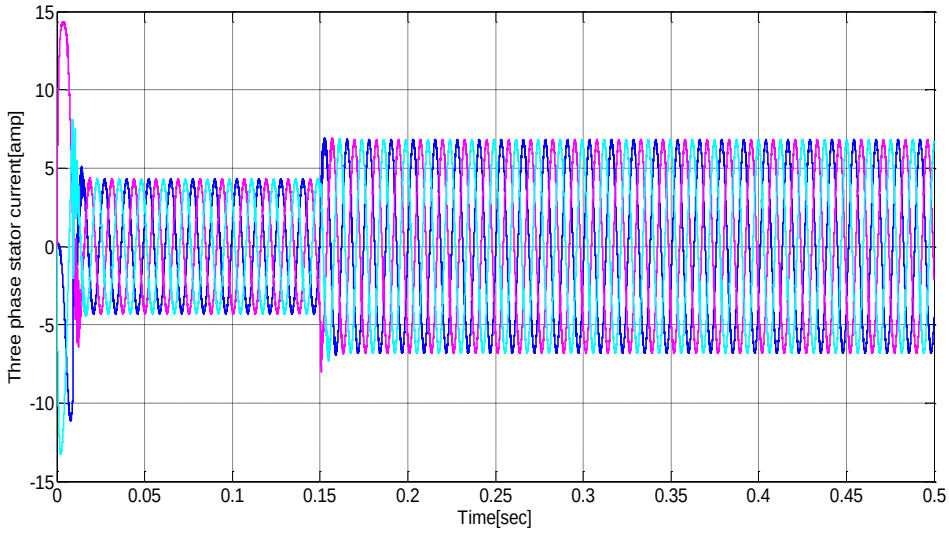


Fig.6.4(c) : Three phase stator current response using DTC- SVM

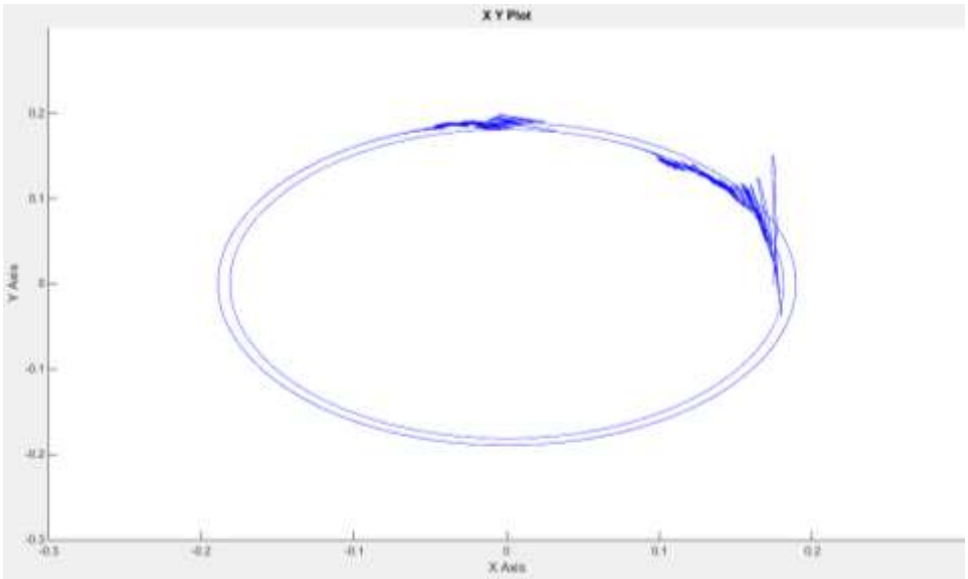


Fig.6.4 (d) : Stator rotor flux response using DTC- SVM

In Fig.6.4 (b) load torque of 20N-m is applied at 0.01 sec of the simulation and removed in 0.15 sec.The electromagnetic torque varies in accordance with the load torque. The reference speed is 500 rpm and there is fluctuation in speed at instant of application or removal of torque though speed practically remains constant. At 0.15 sec speed, three phase stator current &electromagnetic torque is constant with some ripples.

6.3 SIMULATION MODELS OF MATRIX CONVERTER FED PMSM DRIVE

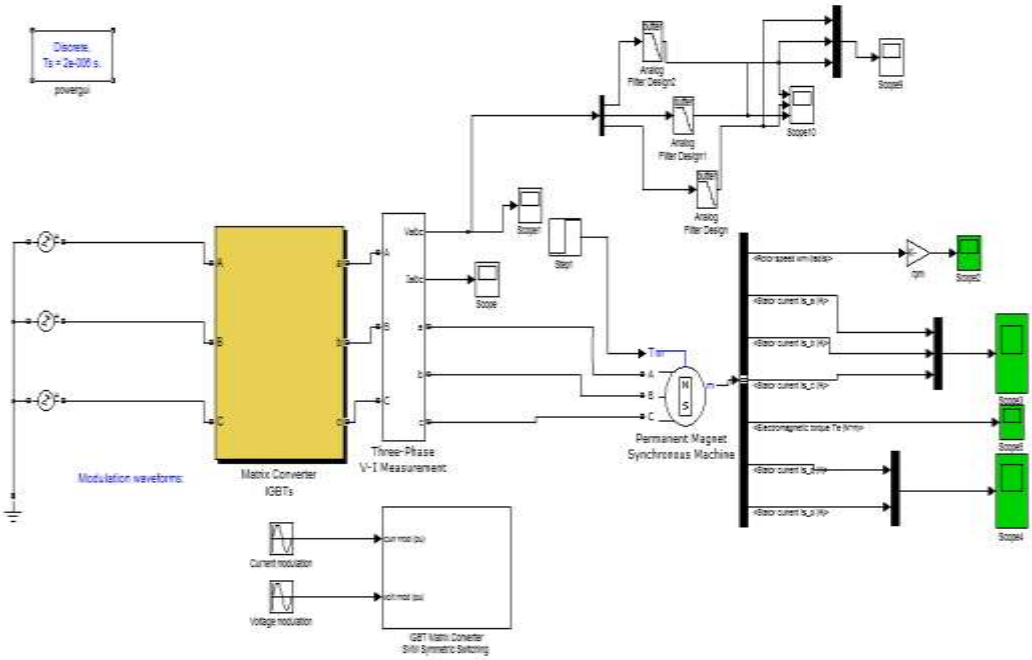


Fig. 6.5 : Simulink model of DTC with Matrix Converter

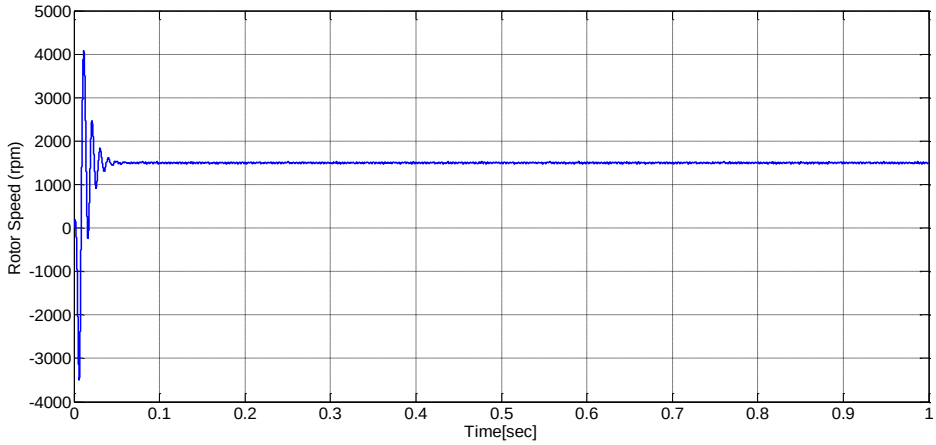


Fig.6.6 (a) : Speed response using Matrix Converter

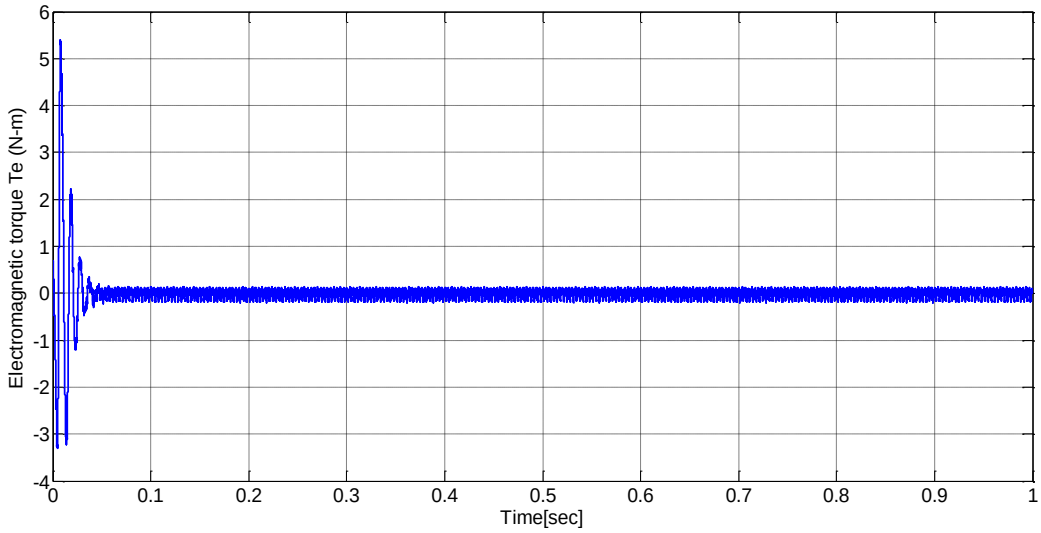


Fig.6.6 (b) : Electromagnetic torque response using Matrix Converter

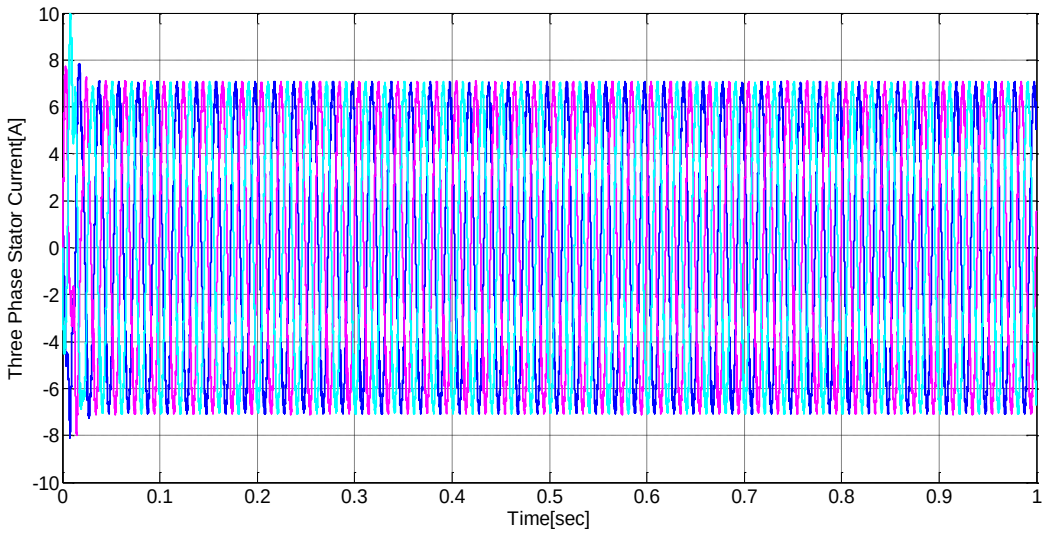


Fig.6.6 (c) : Three phase stator current response using Matrix Converter

In Fig.6.6 (b) load torque of 5 N-m is applied at 0.01 sec of the simulation and removed in 0.03 sec .The electromagnetic torque varies in accordance with the load torque. The reference speed is 500 rpm and there is fluctuation in speed at instant of application or removal of torque though speed practically remains constant. At 0.06 sec speed, three phase stator current &electromagnetic torque is constant with some ripples.

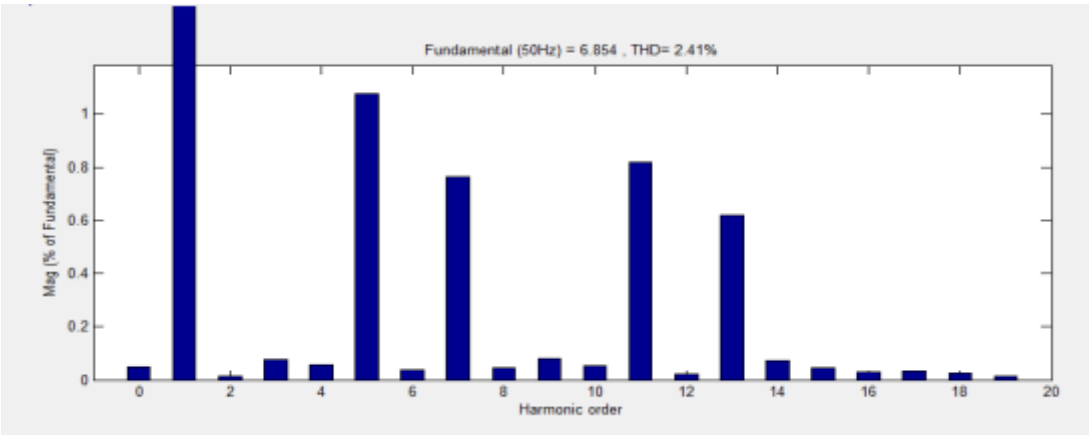


Fig. 6.7 : FFT analysis of DTC with Matrix Converter.

Torque ripples analysis of FOC-SVM, DTC- SVM and DTC with Matrix Converter. Calculated by formula

$$\text{Torque ripple (\%)} = (Tmax - Tmin)/\ Tavg * 100$$

Controller Speed	FOC-SVM	DTC- SVM	DTC with Matrix Converter
500 rpm	28.9538%	30.2601%	18.5449%

Table 6.1 : Torque Ripples analysis

Table 6.2 : Specification of PMSM for two level inverter

Sr. No.	PMSM Parameter	Value
1.	Stator Resistance Rs	2.885Ω
2.	d-axis Inductance Ld	$8.5x10^{-3}$H
3.	q-axis Inductance Lq	$8.5x10^{-3}$ H
4.	Permanent Magnet Flux	0.185Wb
5.	No of Pole pairs	4
6.	Torque	0.051Nm
8.	Movement of Inertia(J)	$2.26x10^{-5}$Kg/m^2
8.	Viscous coefficient(f)	$1.349x10^{-5}$Nms

6.4 SIMULATION MODEL OF THREE LEVEL DIODE CLAMPED INVERTER FED PMSM DRIVE USING FOC-PWM

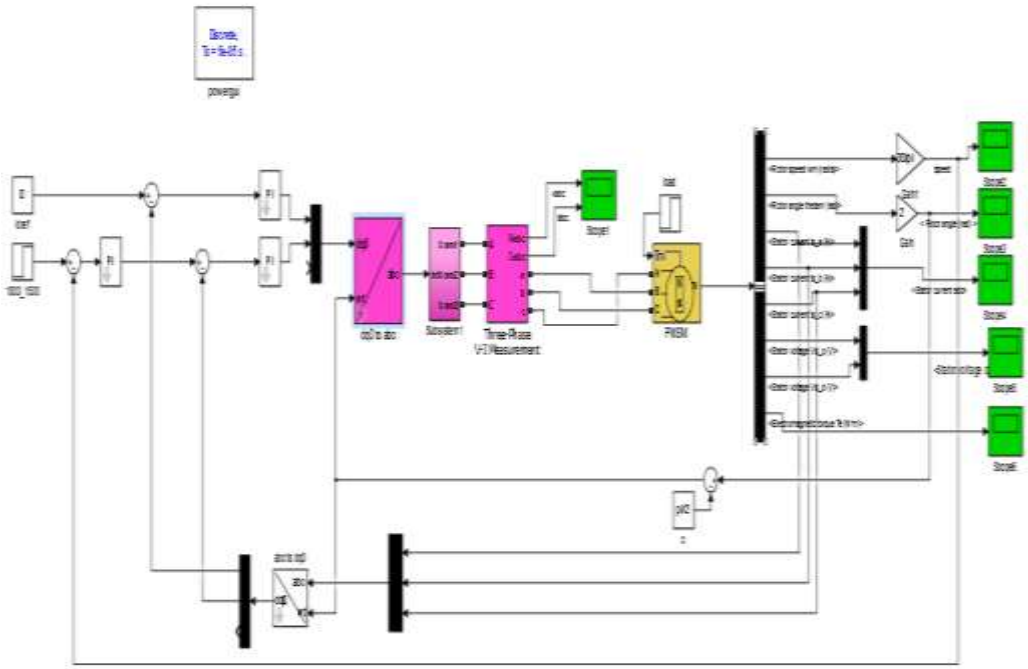


Fig.6.8 : Simulation Model of three level DCMLI fed PMSM drive using PWM

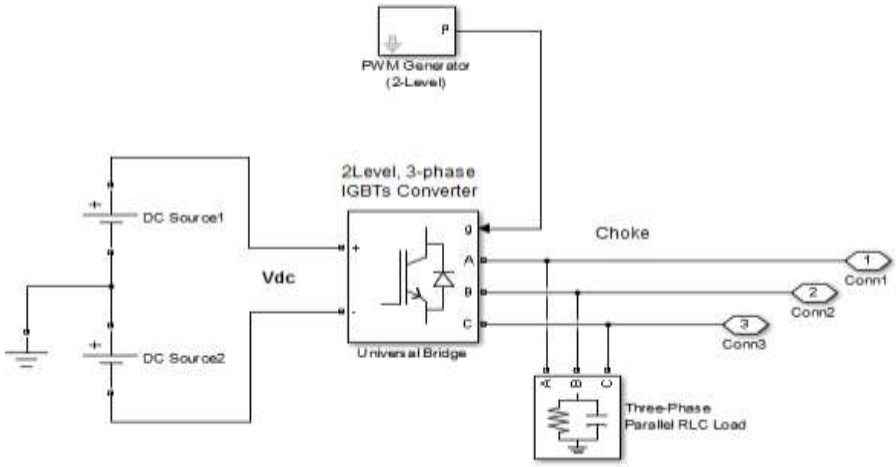


Fig. 6.9 : Simulation Model of PWM inverter

6.5 SIMULATION MODEL OF THREE LEVEL DIODE CLAMPED INVERTER FED PMSM DRIVE USING FOC-SVM

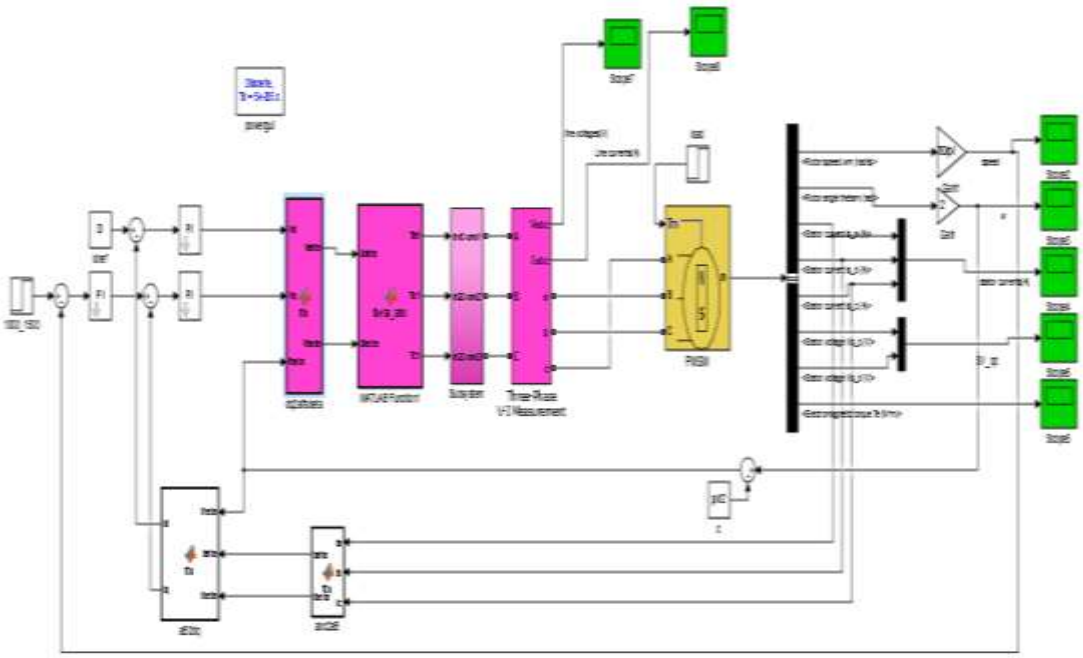


Fig. 6.10 : Simulation Model of three level DCMLI fed PMSM drive using SVM

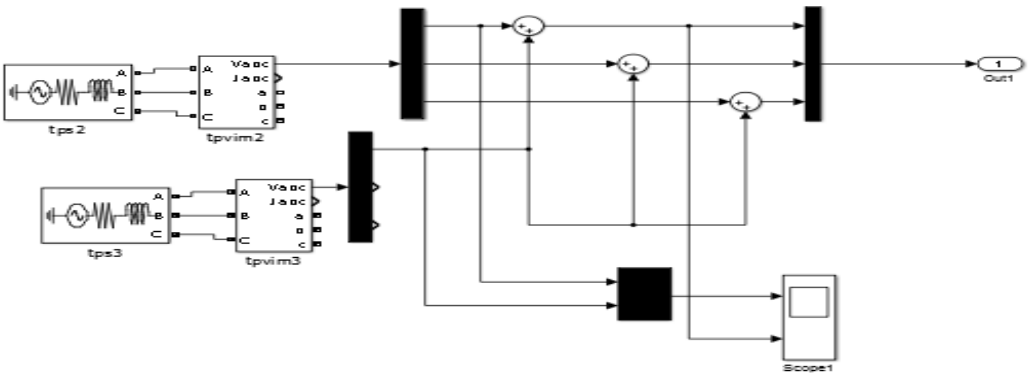


Fig. 6.11 : Simulation Model of SV-PWM inverter

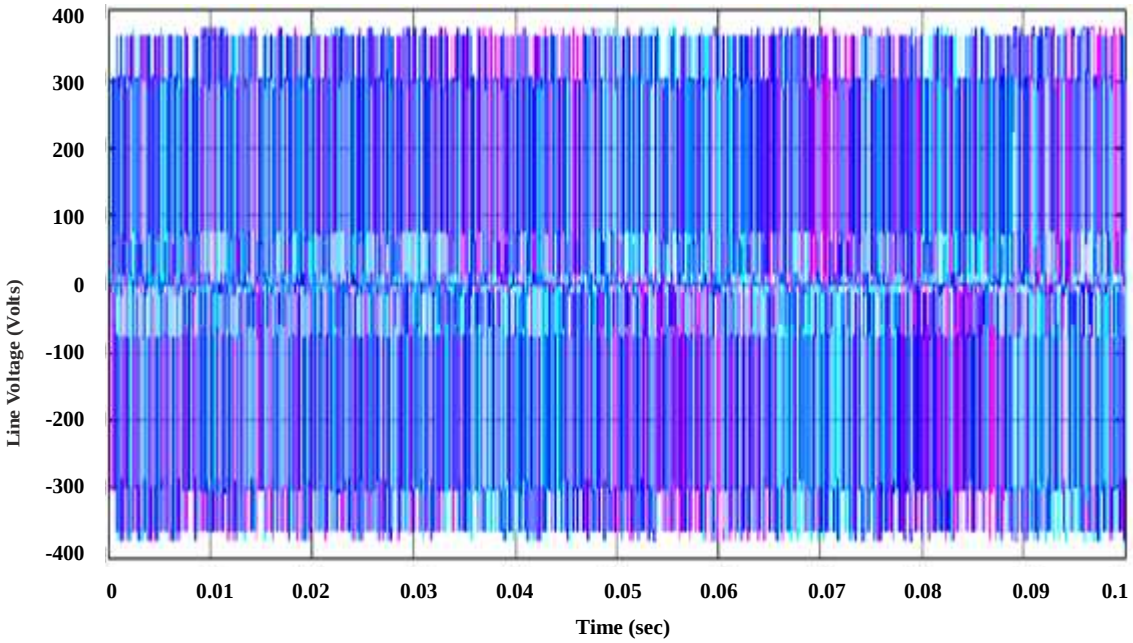


Fig.6.12 (a) : Inverter line voltage waveform using FOC- PWM

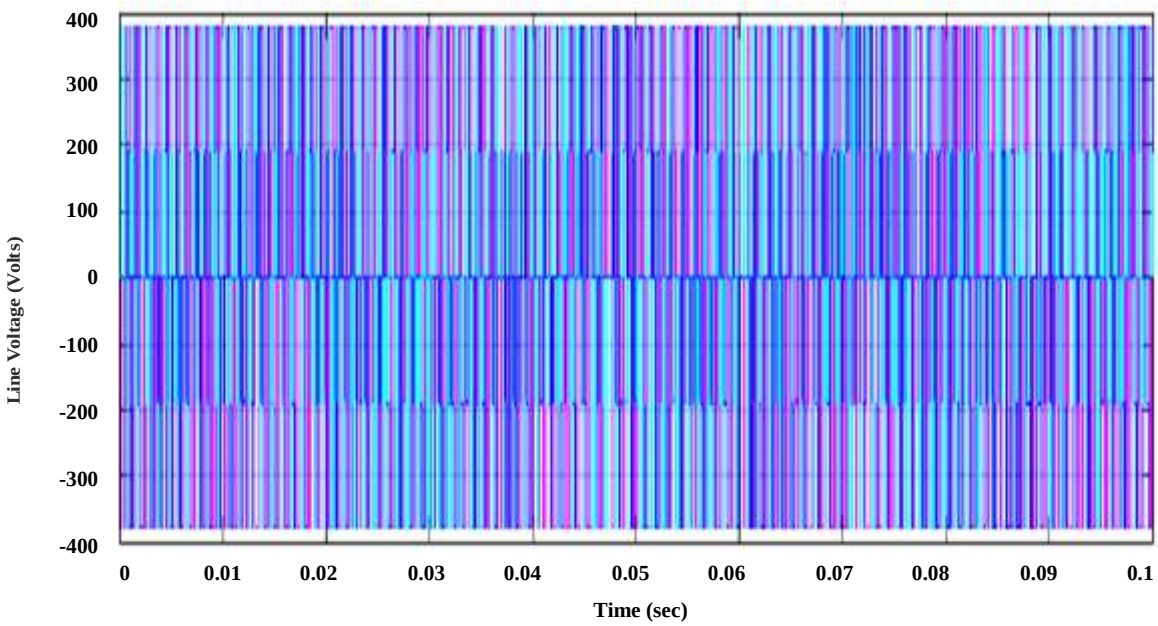


Fig. 6.12.(b) : Inverter line voltage waveform using FOC-SVM

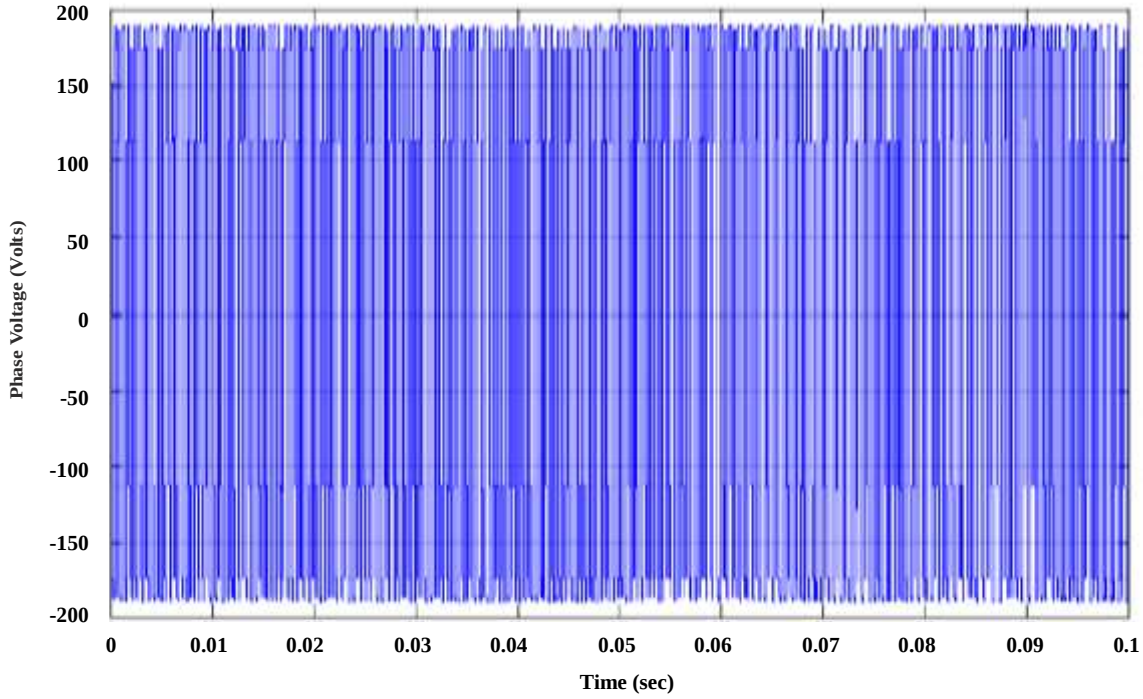


Fig.6.13 (a) : Inverter phase voltage waveform using FOC- PWM

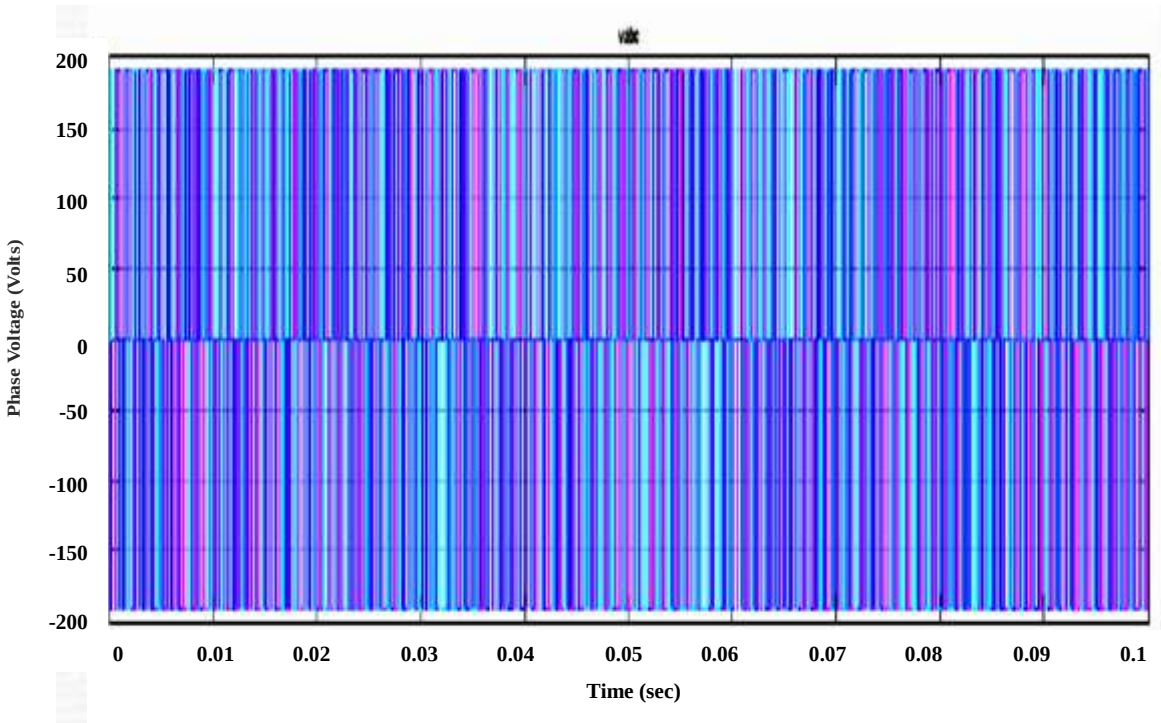


Fig. 6.13(b) : Inverter phase voltage waveform using FOC-SVM

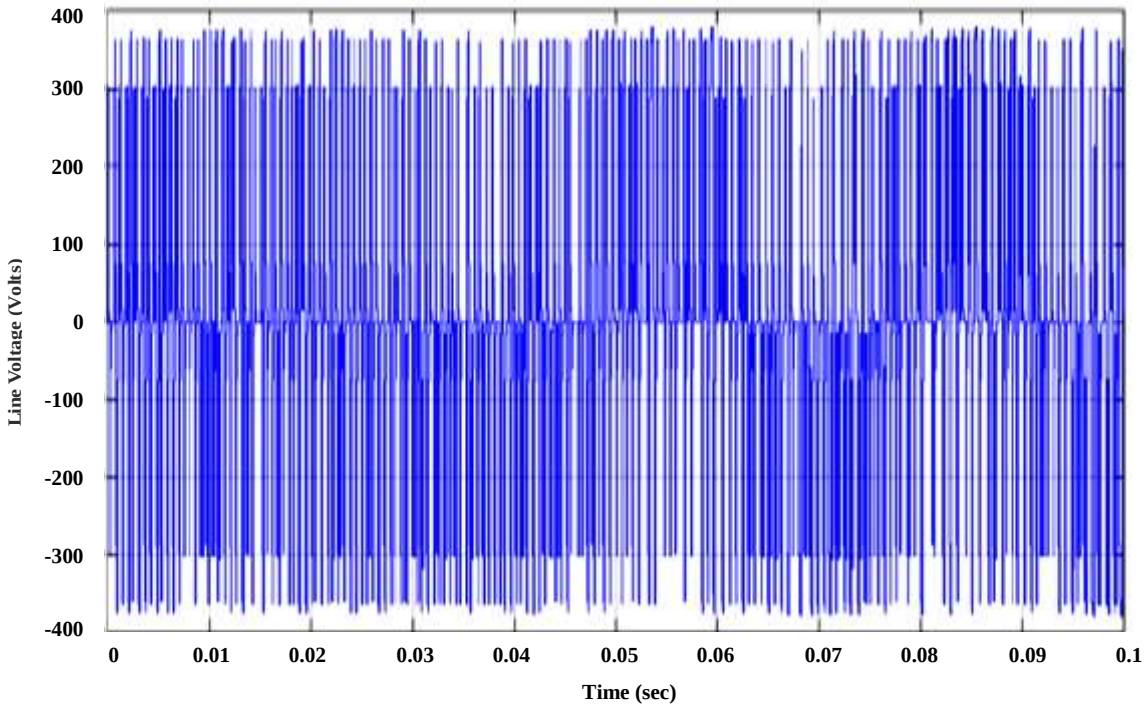


Fig.6.14 (a) : Single phase inverter line voltage waveform using FOC- PWM

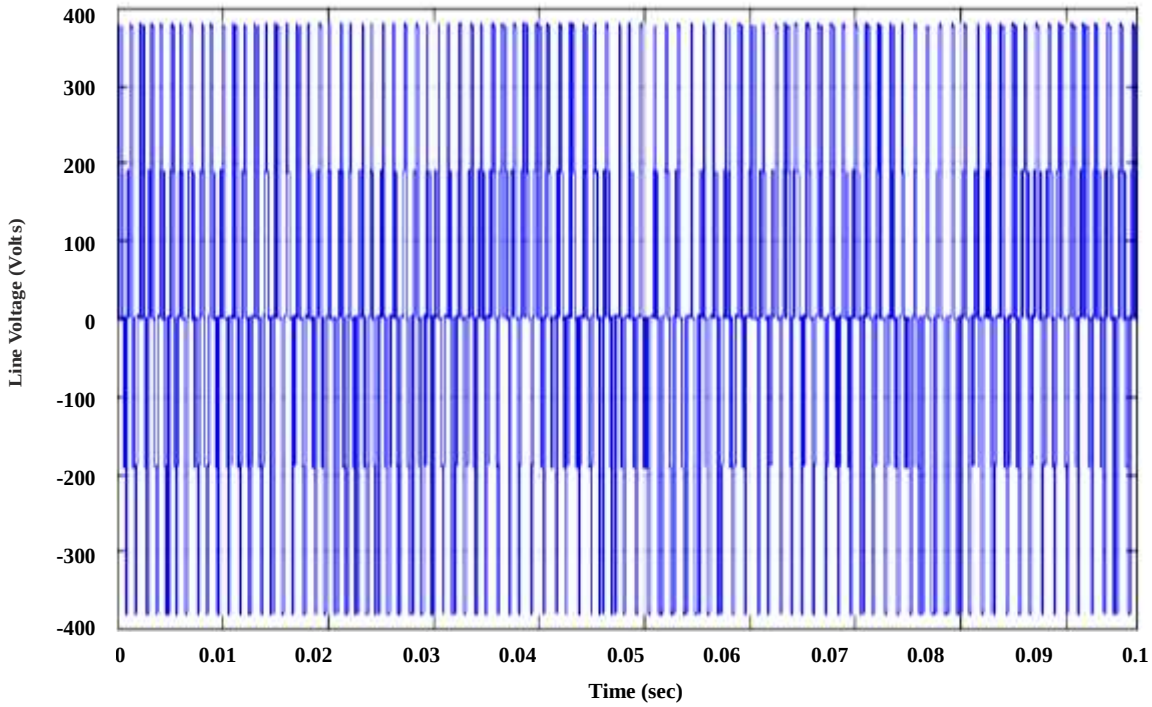


Fig.6.14 (b) : Single phase inverter line voltage waveform using FOC-SVM

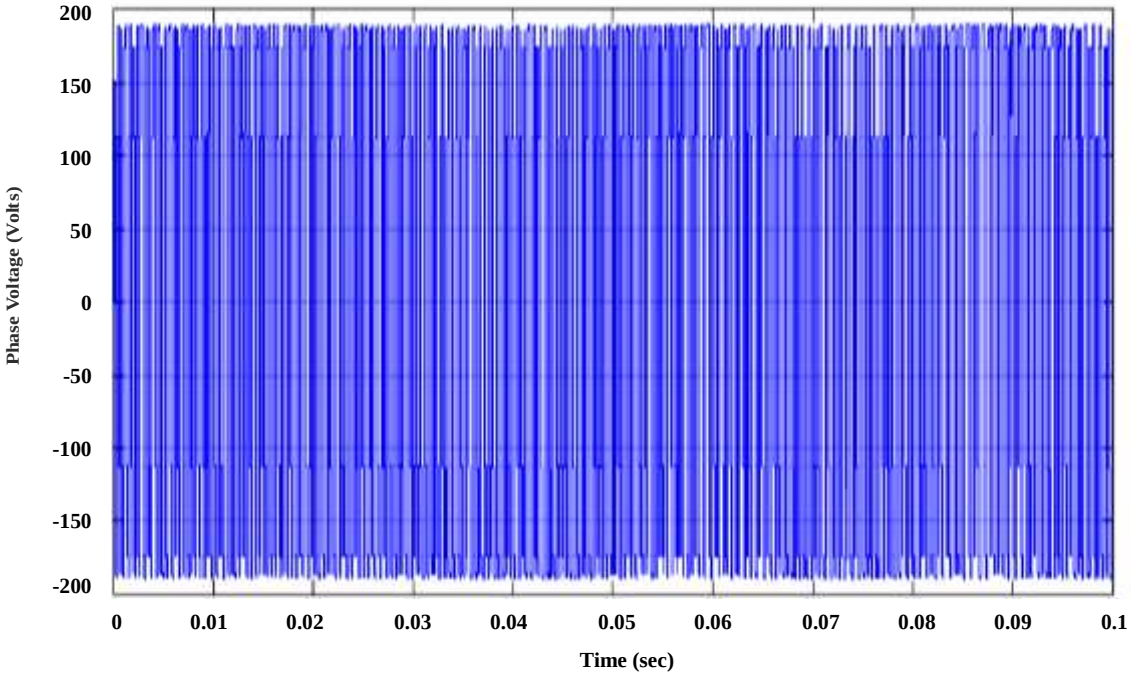


Fig.6.15 (a) : Single phase inverter phase voltage waveform using FOC- PWM

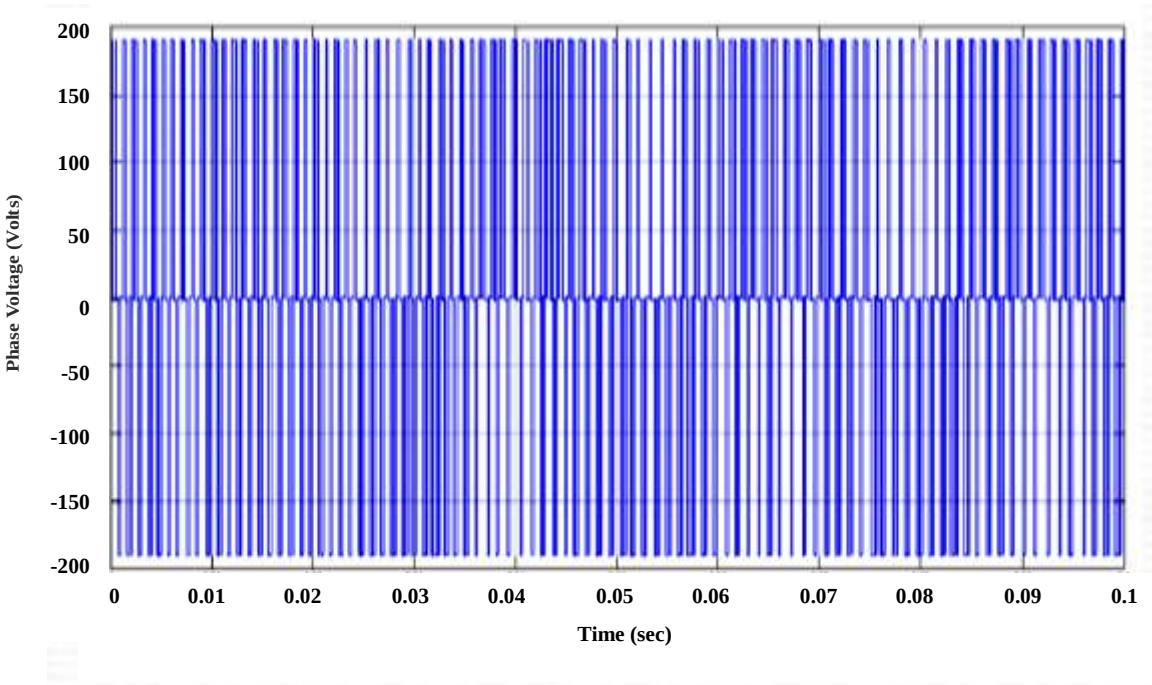


Fig.6.15 (b) : Single phase inverter phase voltage waveform using FOC-SVM

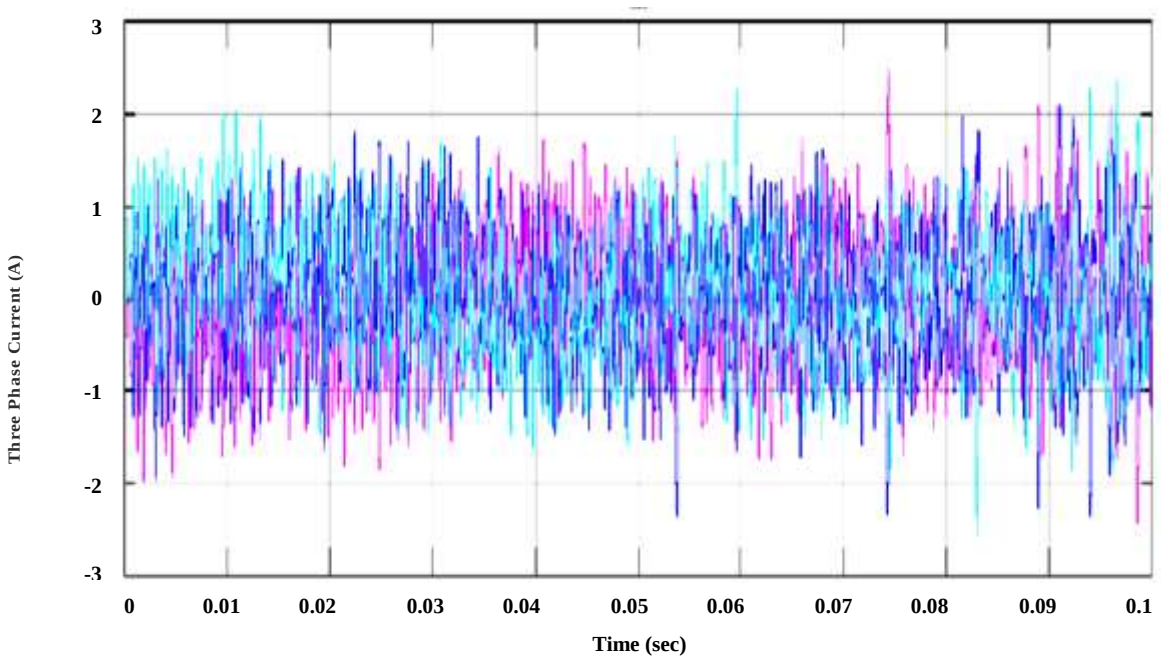


Fig. 6.16 (a) : Three phase current waveform using FOC- PWM

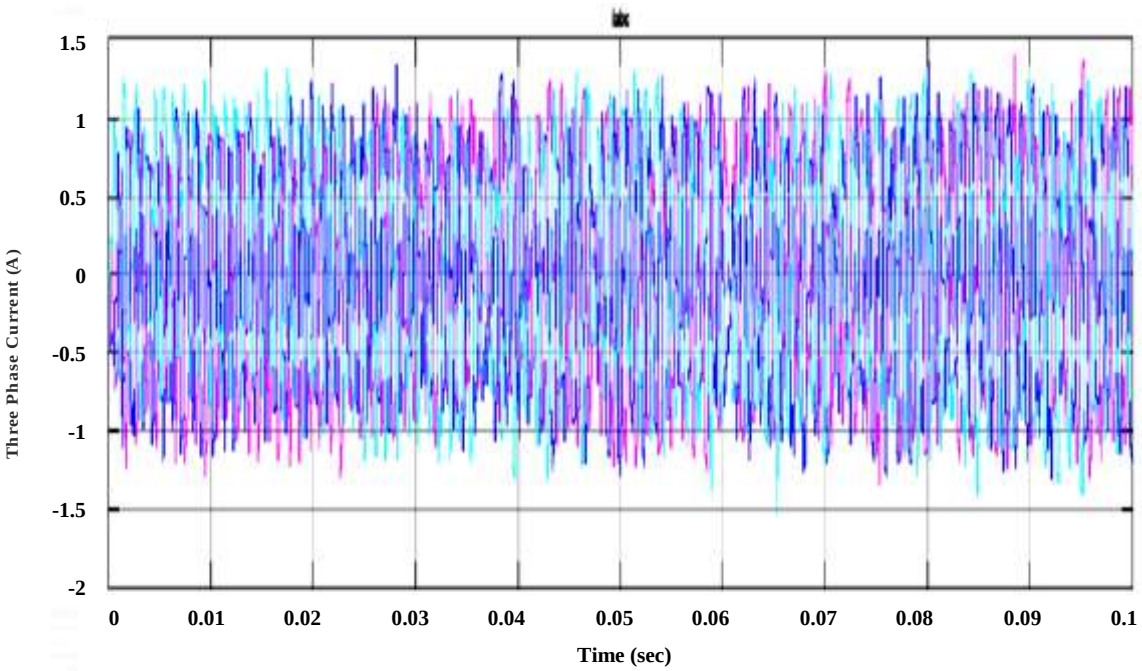


Fig.6.16 (b) : Three phase current waveform using FOC-SVM

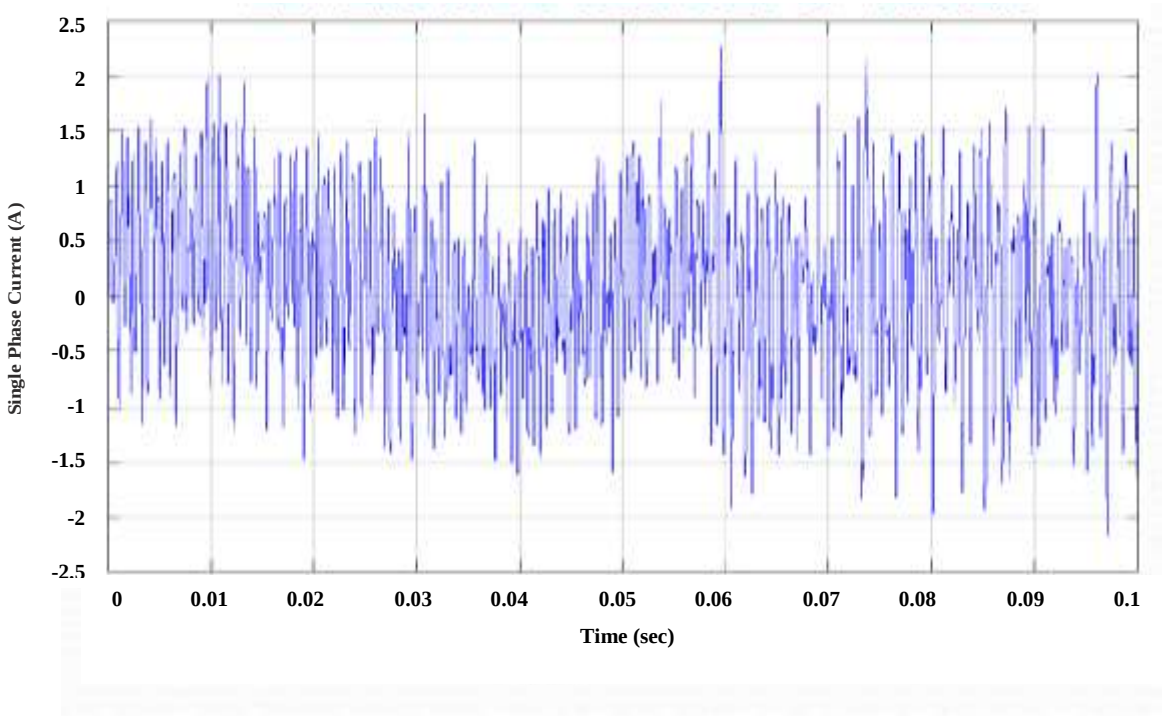


Fig.6.17 (a) : Single phase current waveform using FOC- PWM

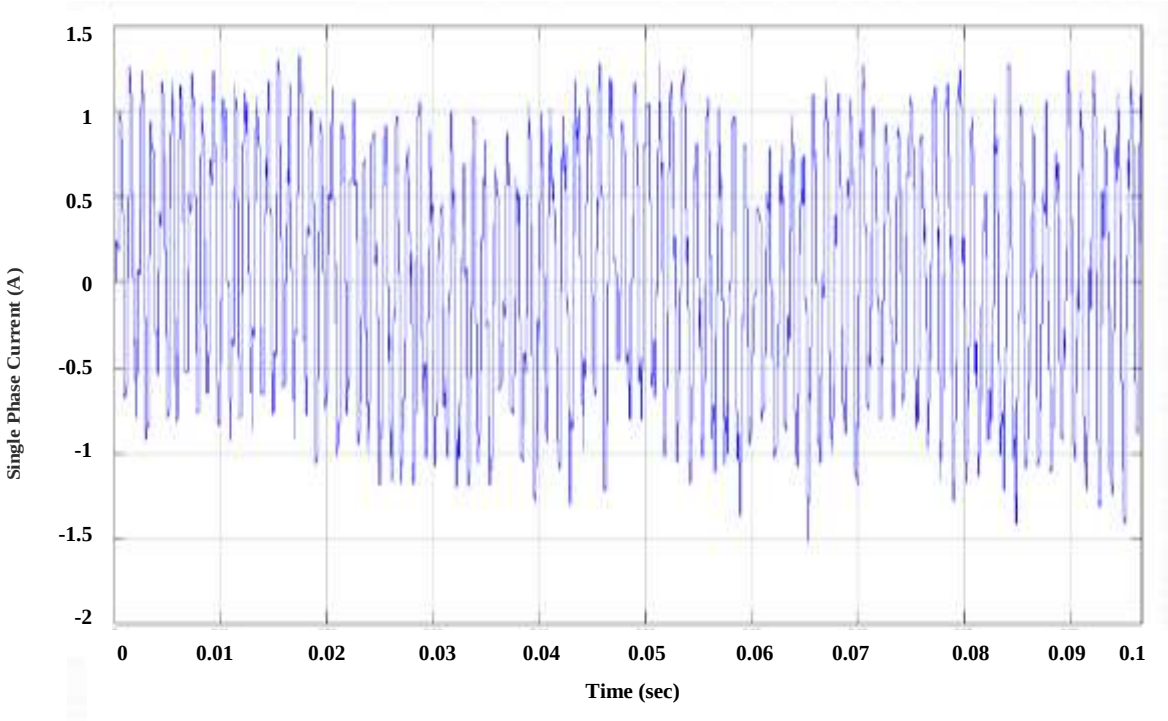


Fig.6.17 (b) : Single phase current waveform using FOC-SVM

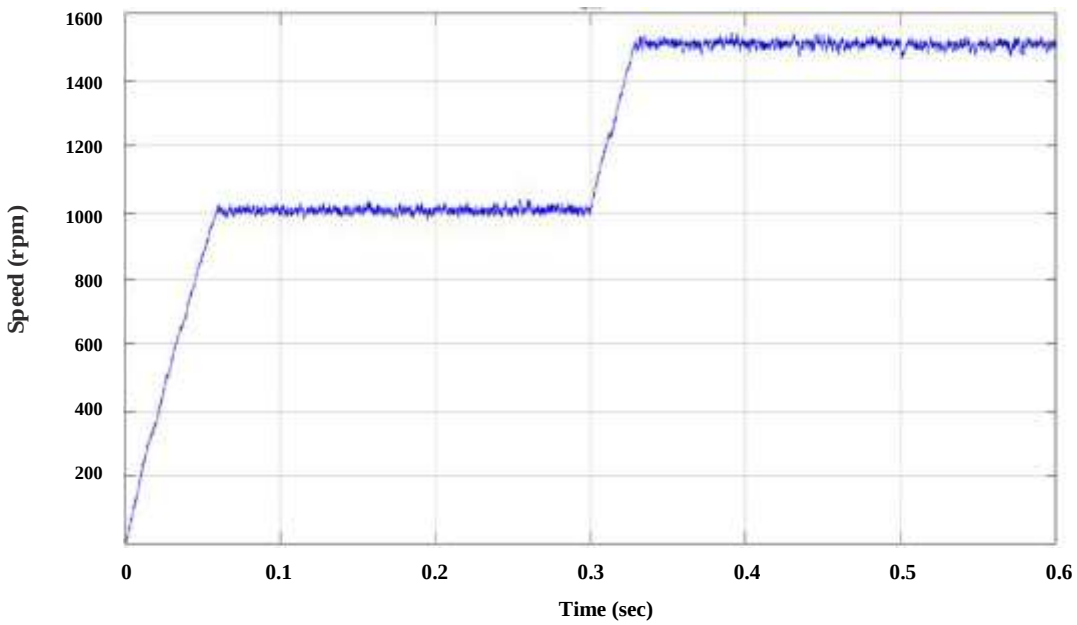


Fig. 6.18.(a) : Output speed response using FOC- PWM

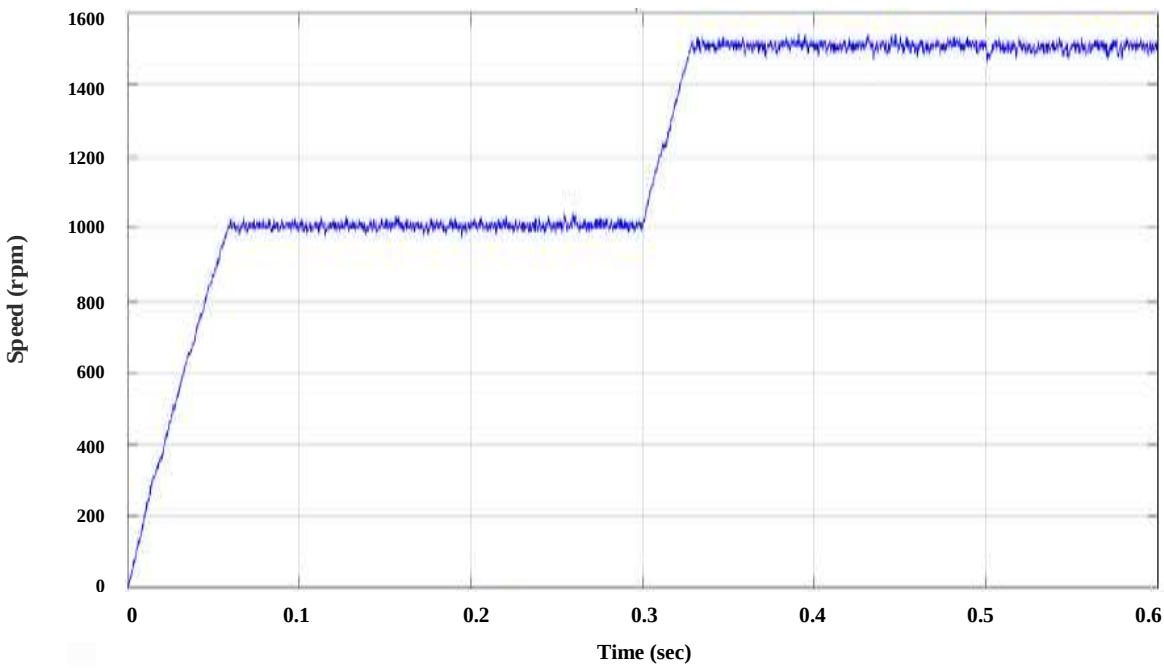


Fig. 6.18 (b) : Output speed response using FOC-SVM

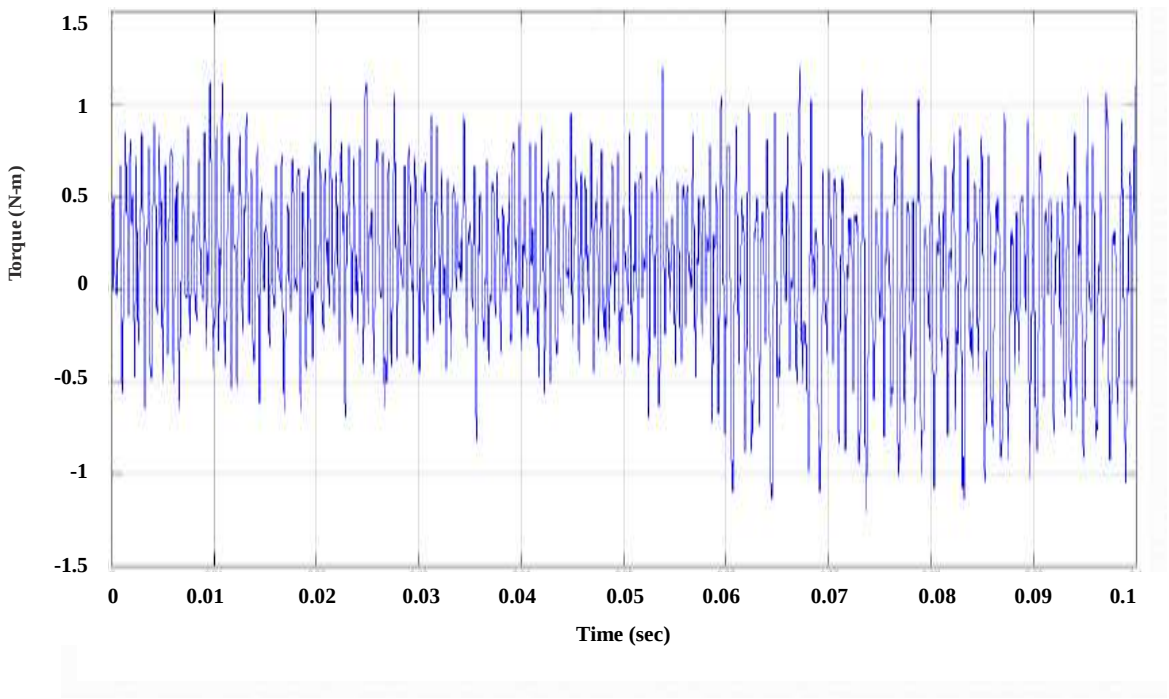


Fig. 6.19 (a) : Output torque response using FOC- PWM

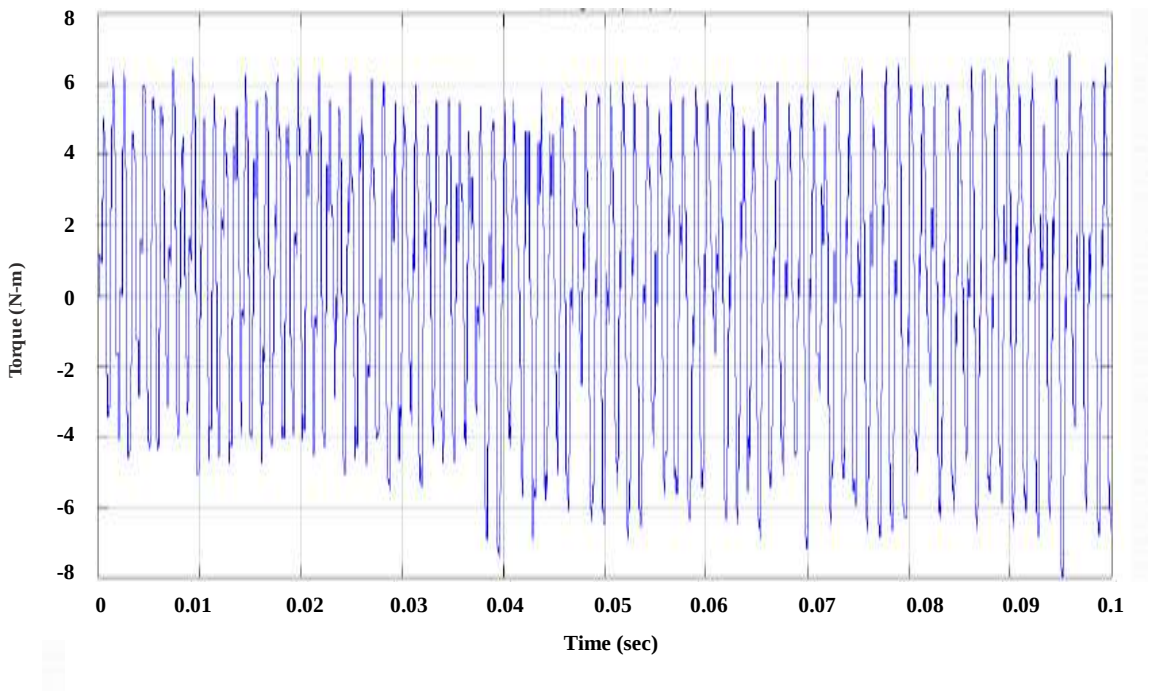


Fig. 6.19 (b) : Output torque response using FOC-SVM

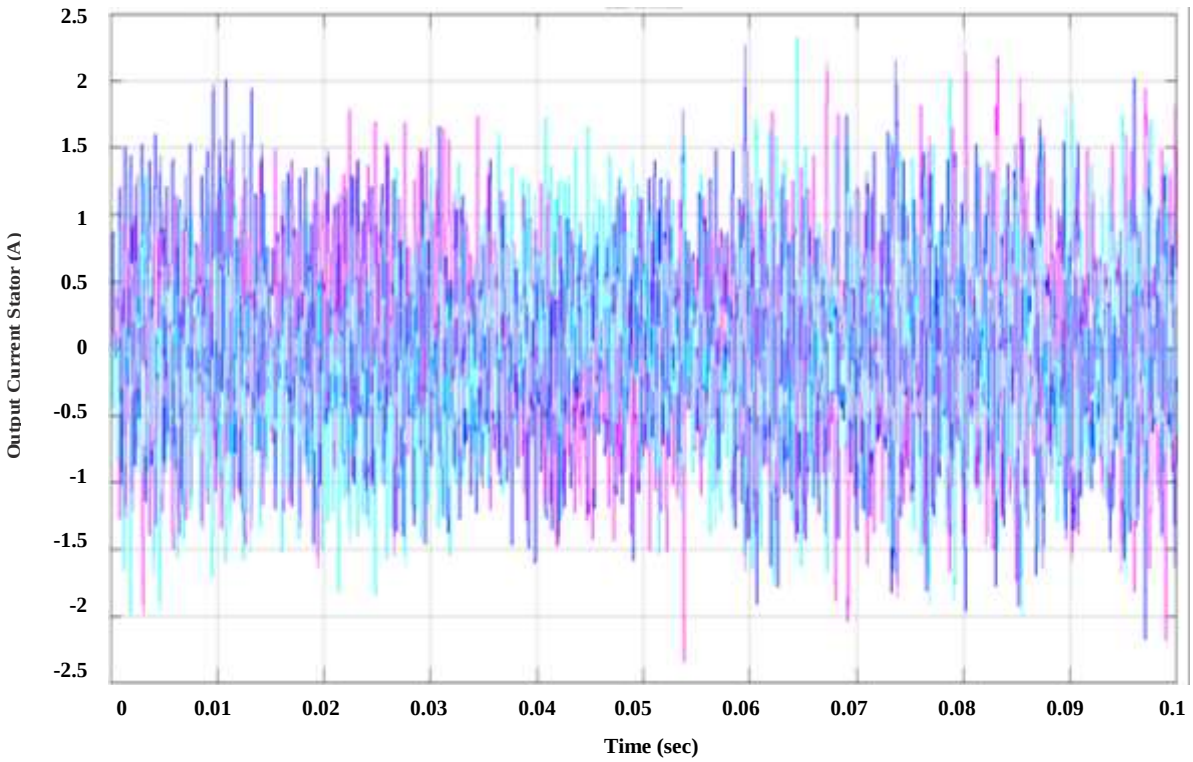


Fig.6.20 (a) : Output stator current response using FOC- PWM

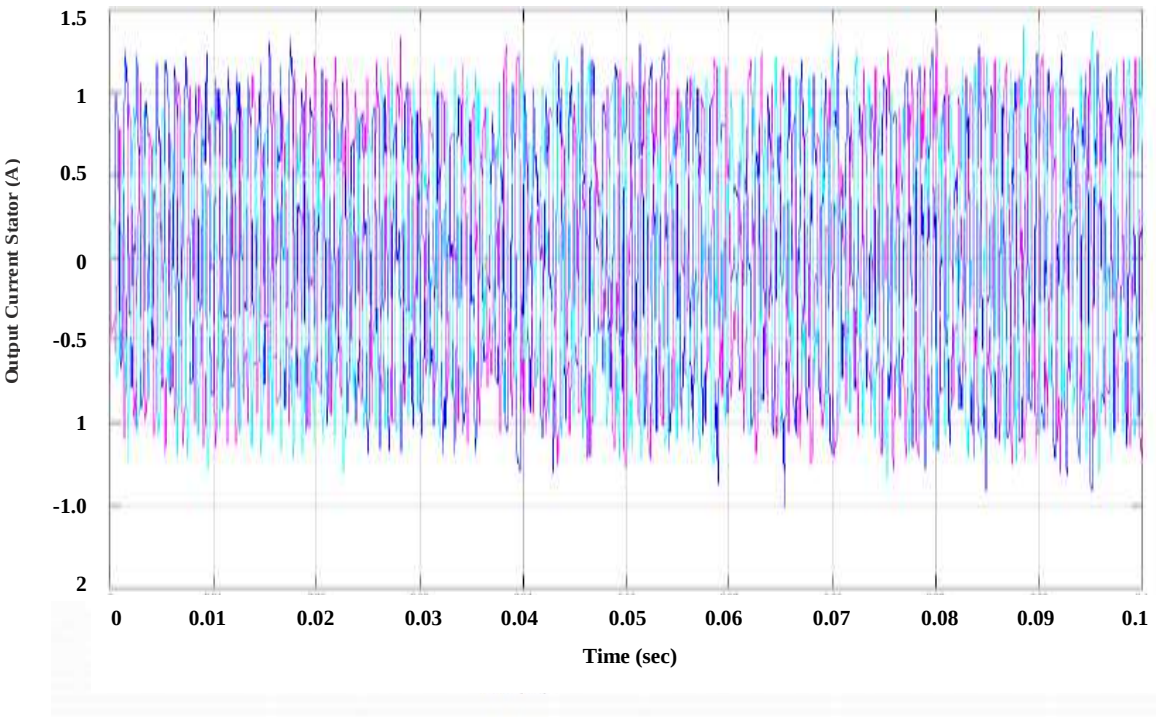


Fig.6.20 (b) : Output stator current response using FOC-SVM

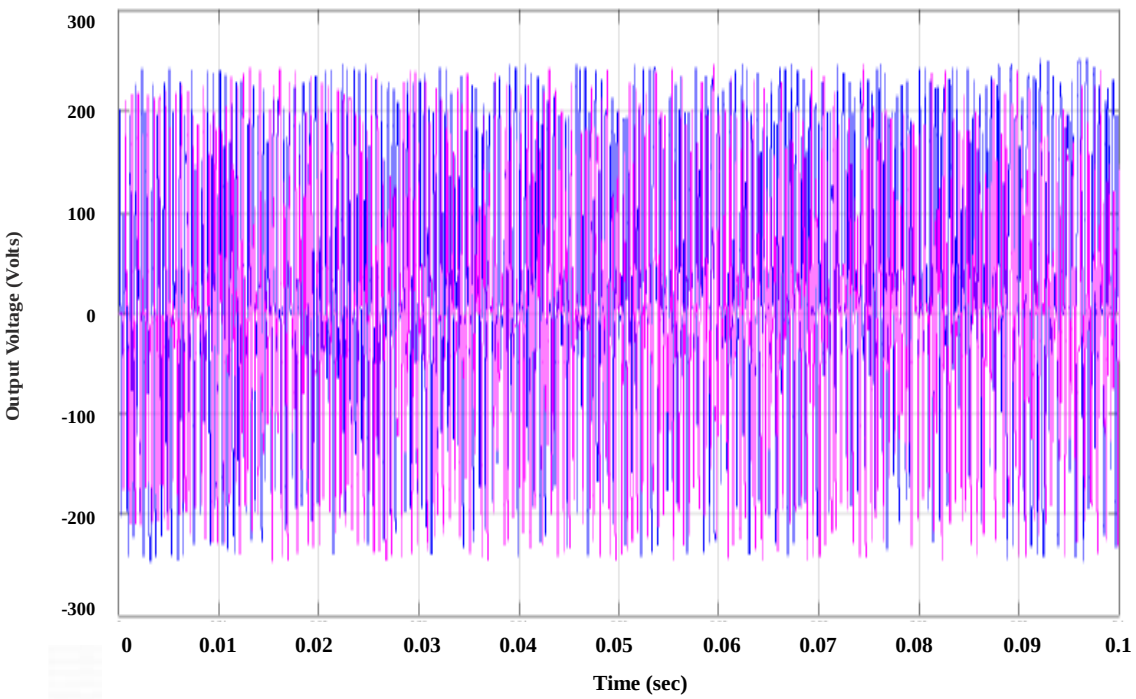


Fig.6.21 (a) : Output motor voltage response using FOC- PWM

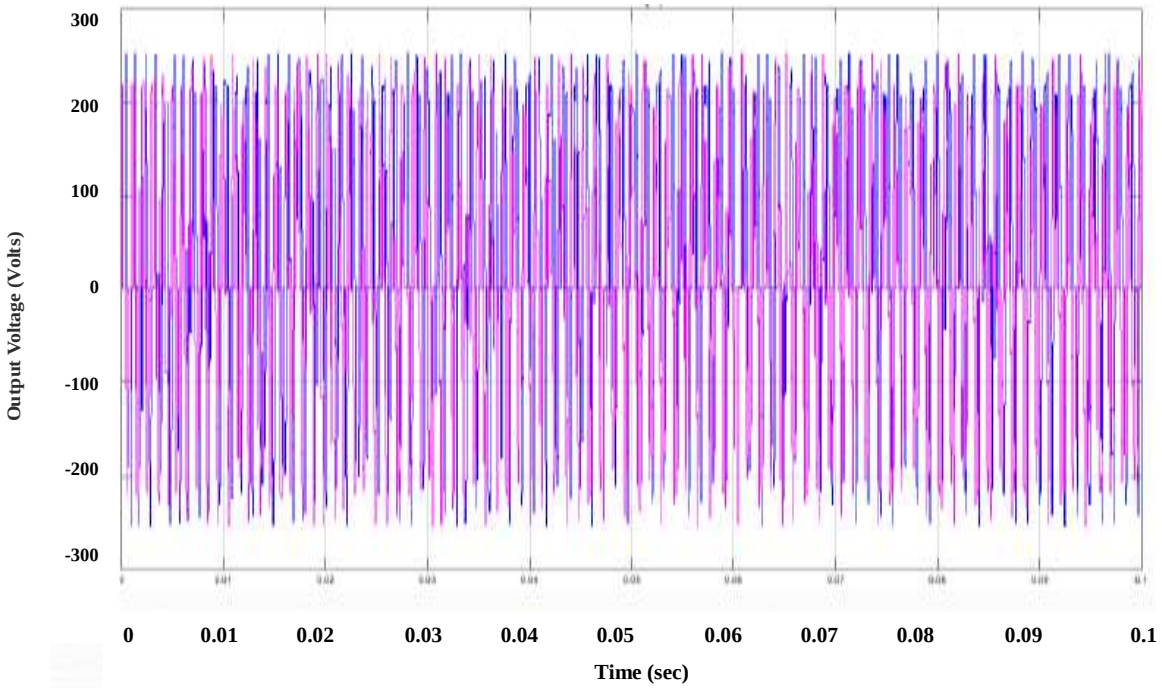


Fig.6.21 (b) : Output motor voltage response using FOC-SVM

6.6 SIMULATION MODEL OF THREE LEVEL DIODE CLAMPED INVERTER FED PMSM DRIVE USING FOC-CBSVM

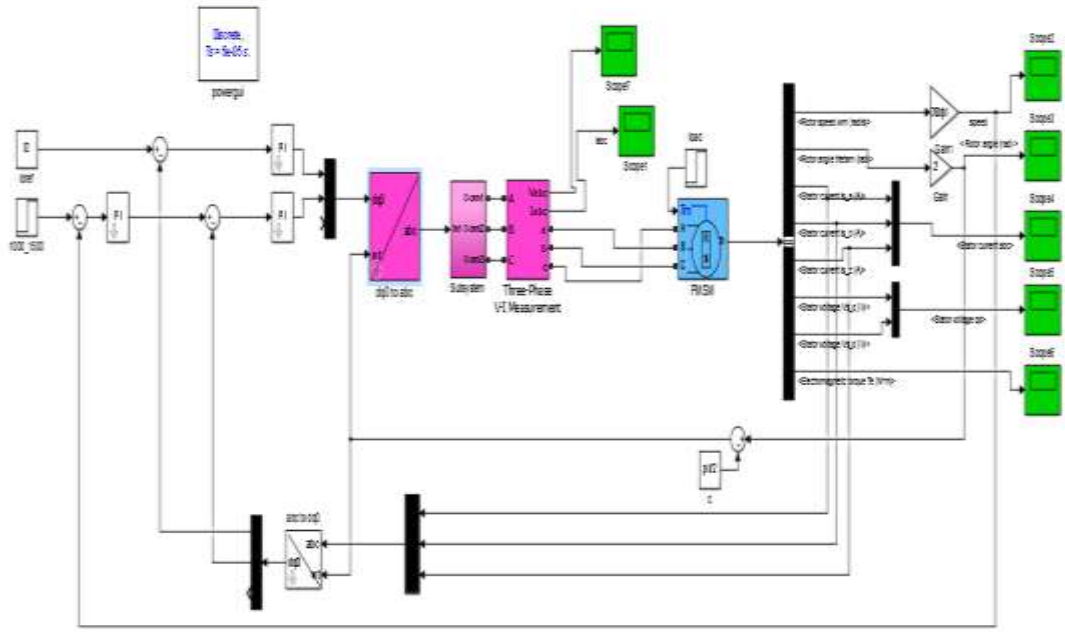


Fig. 6.22. : Simulation Model of three level diode clam

ped inverter fed PMSM drive using FOC- CBSVM

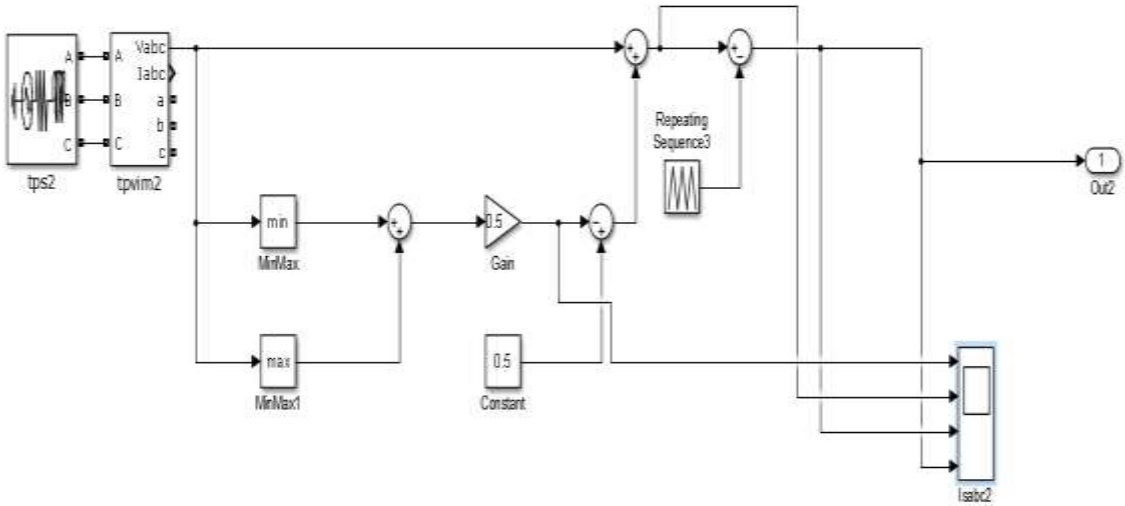


Fig. 6.23 : Simulation Model of CB-SVPWM inverter

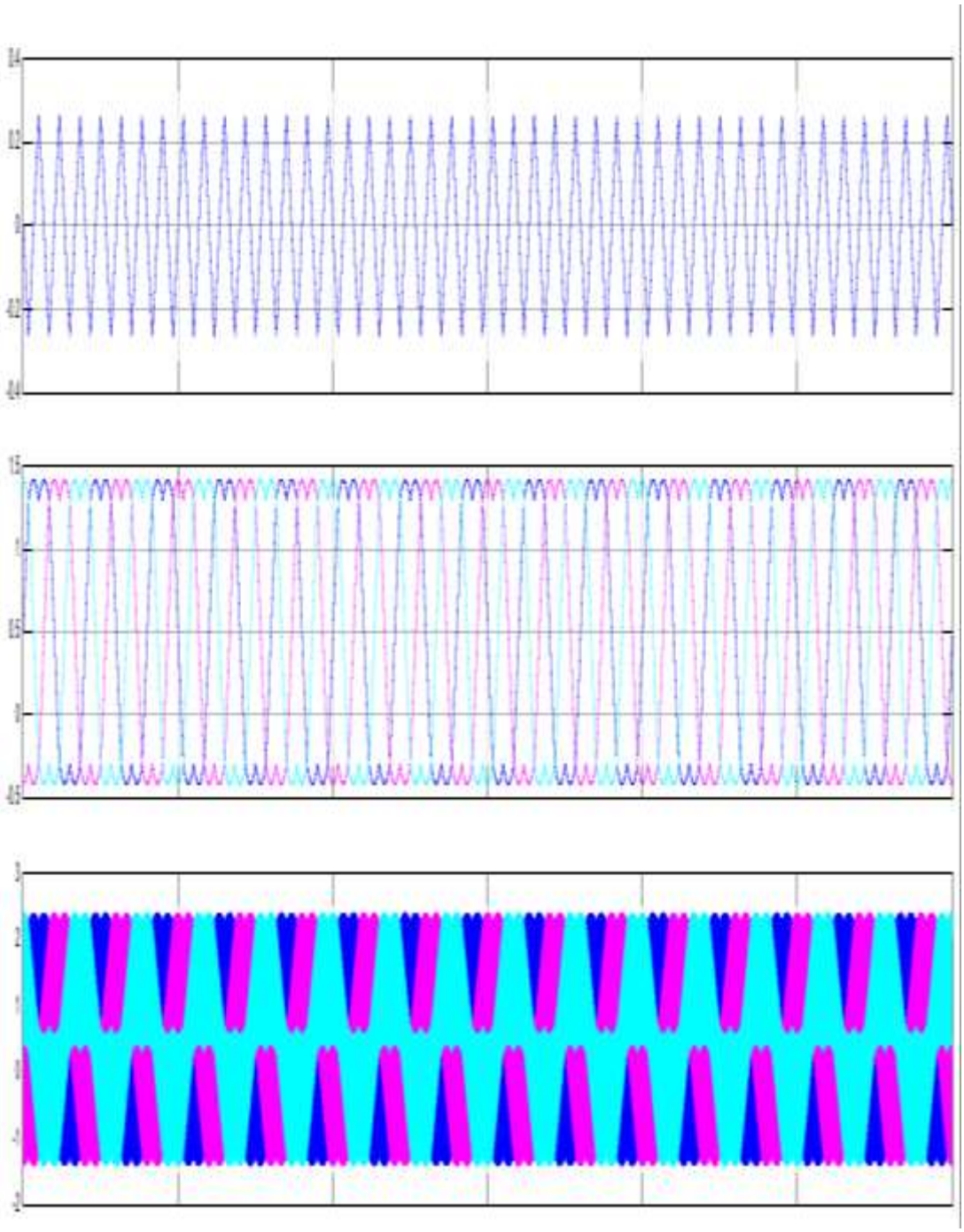


Fig. 6.24 : Output waveforms of CB-SVPWM inverter

6.7 SIMULATION MODEL OF THREE LEVEL DIODE CLAMPED INVERTER FED PMSM DRIVE USING DTC-CBSVPWM

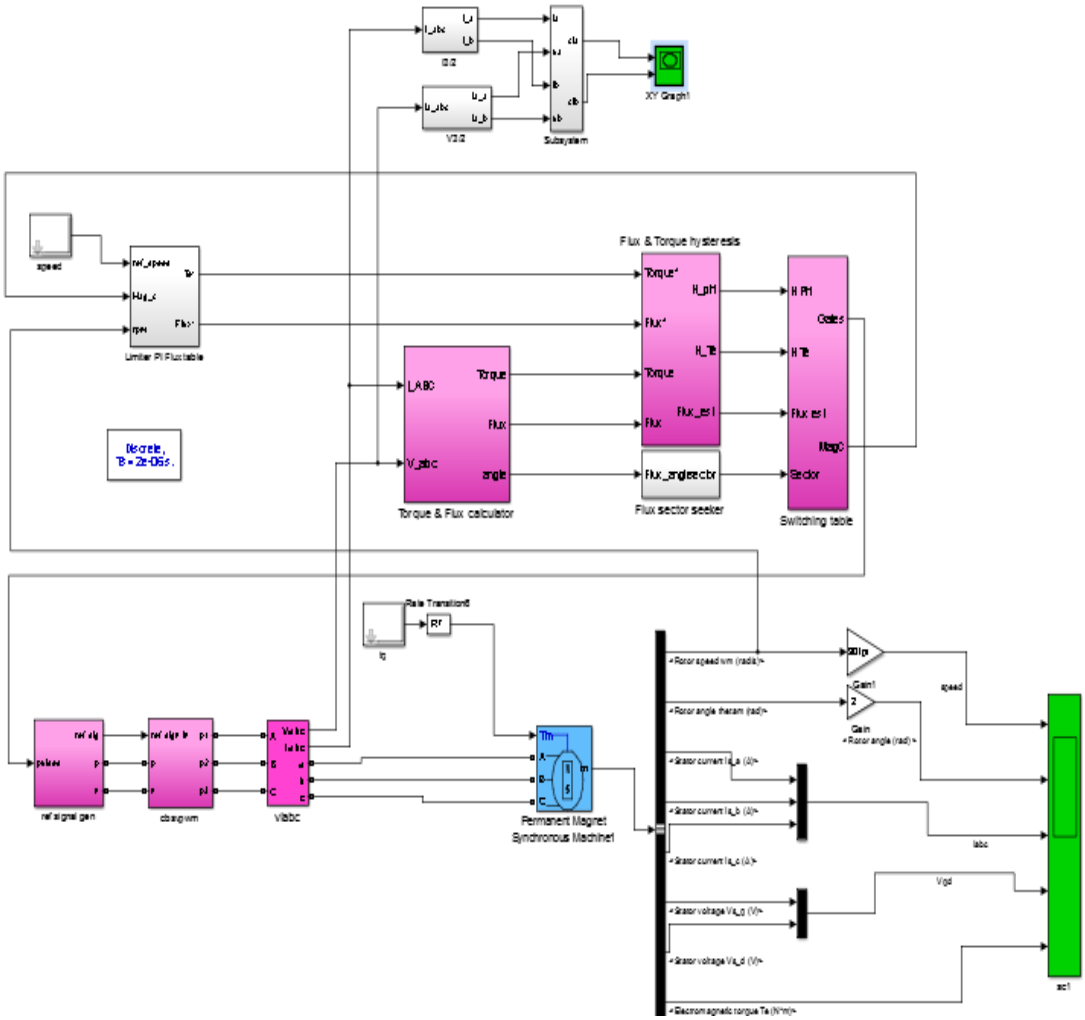


Fig. 6.25 : Simulation Model of three level diode clamped inverter fed PMSM drive with DTC-CBSVM

6.8 STEADY STATE PERFORMANCE OF FOC–DTC-CBSVM

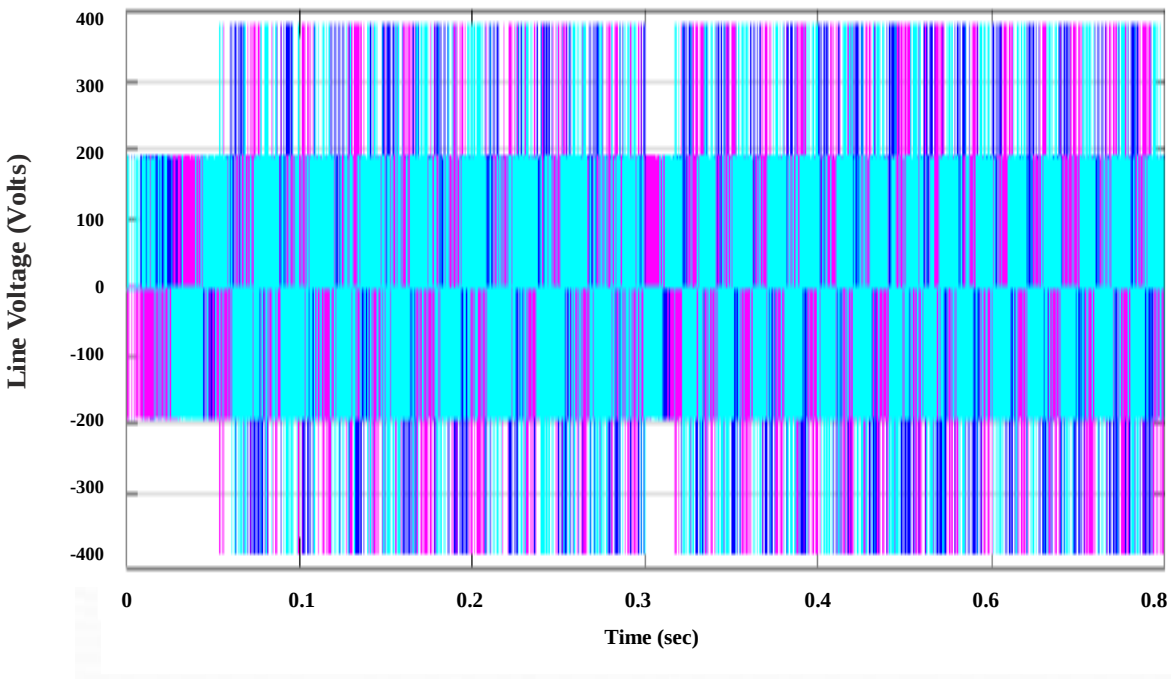


Fig. 6.26(a) : Three phase inverter line voltage waveform using FOC- CBSVPWM

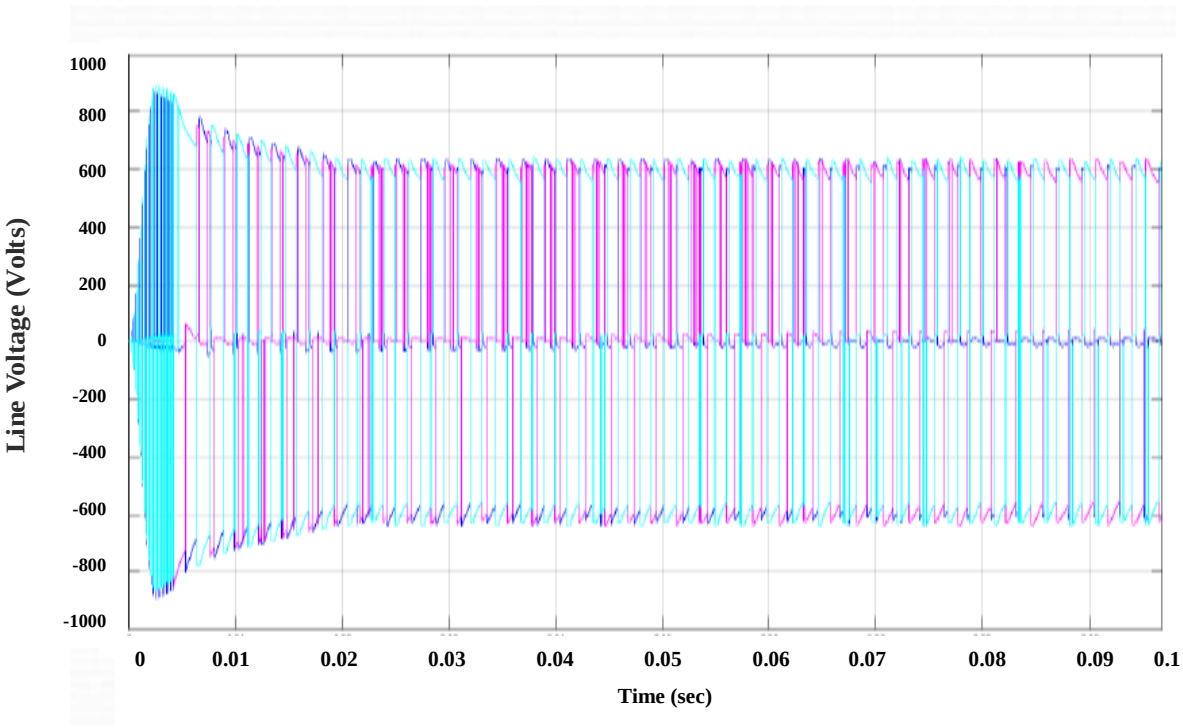


Fig. 6.26(b) : Three phase inverter line voltage waveform using DTC- CBSVPWM

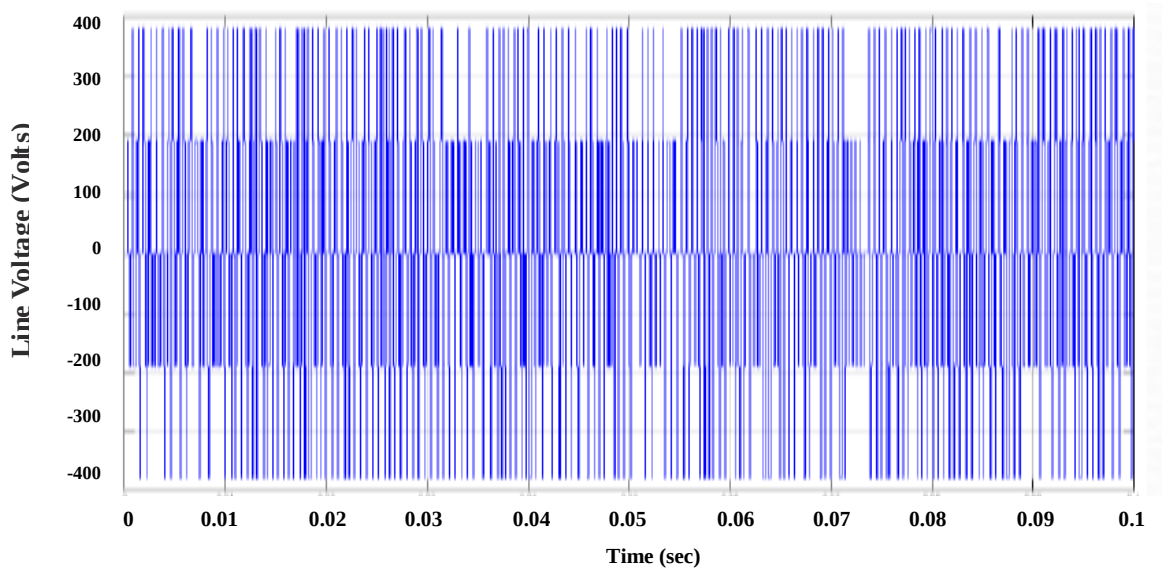


Fig.6.27 (a) : Single phase inverter line voltage waveform using FOC- CBSVPWM

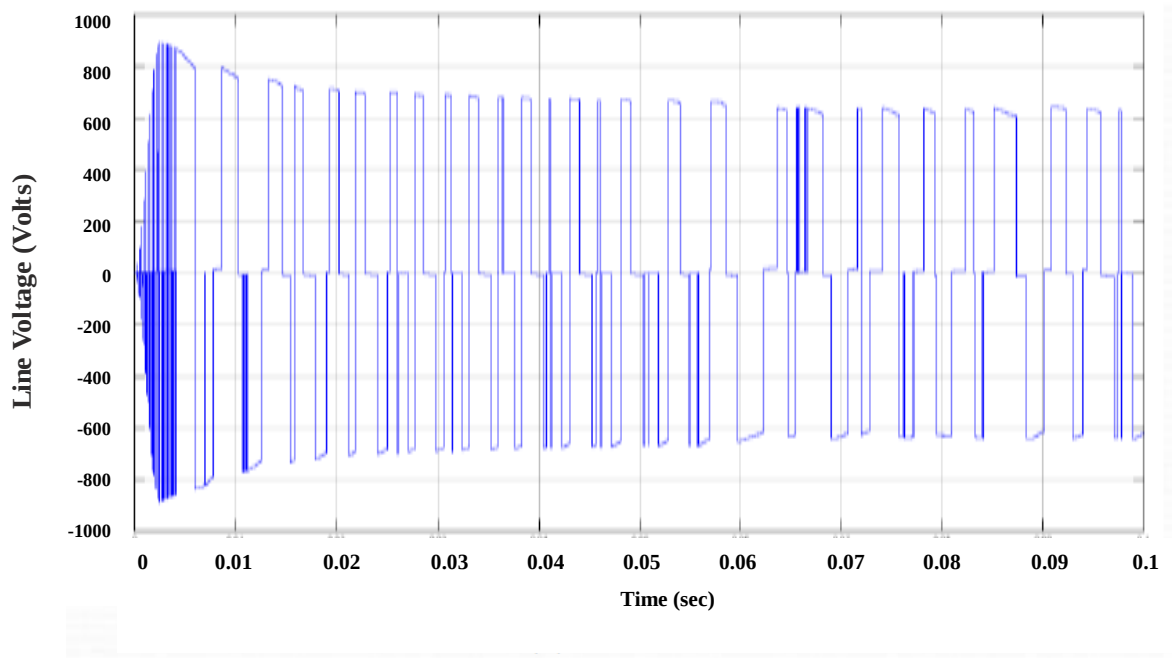


Fig. 6.27(b) : Single phase inverter line voltage waveform using DTC- CBSVPWM

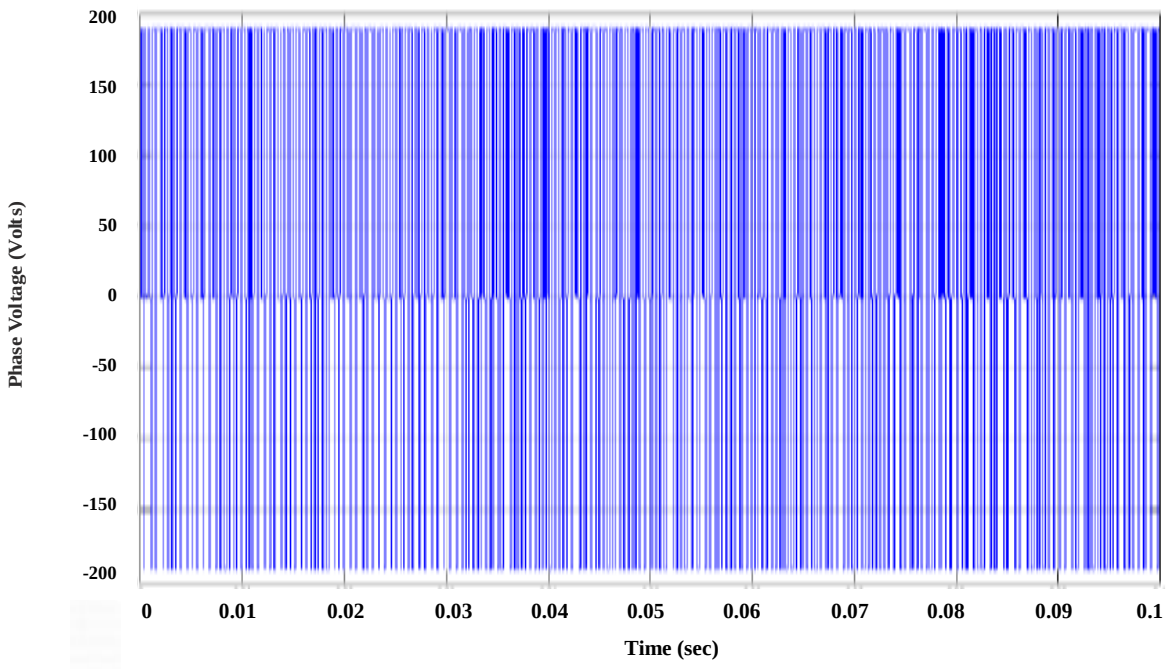


Fig.6.28 (a) : Single phase inverter voltage waveform using FOC- CBSVPWM

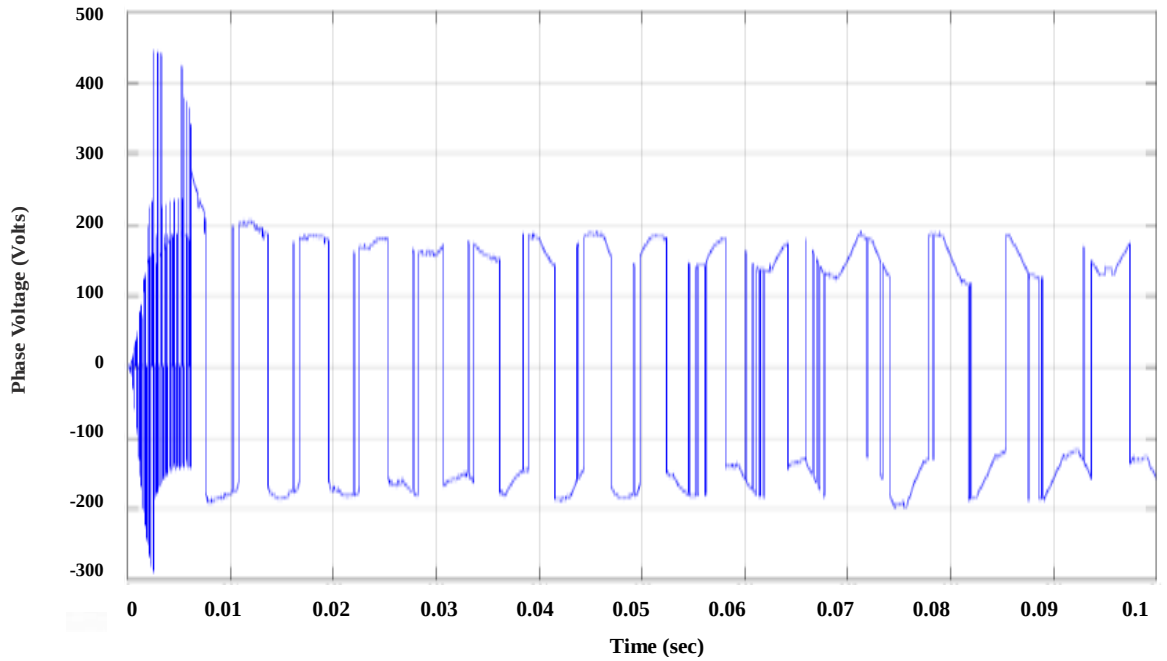


Fig. 6.28 (b) : Single phase inverter voltage waveform using DTC- CBSVPWM

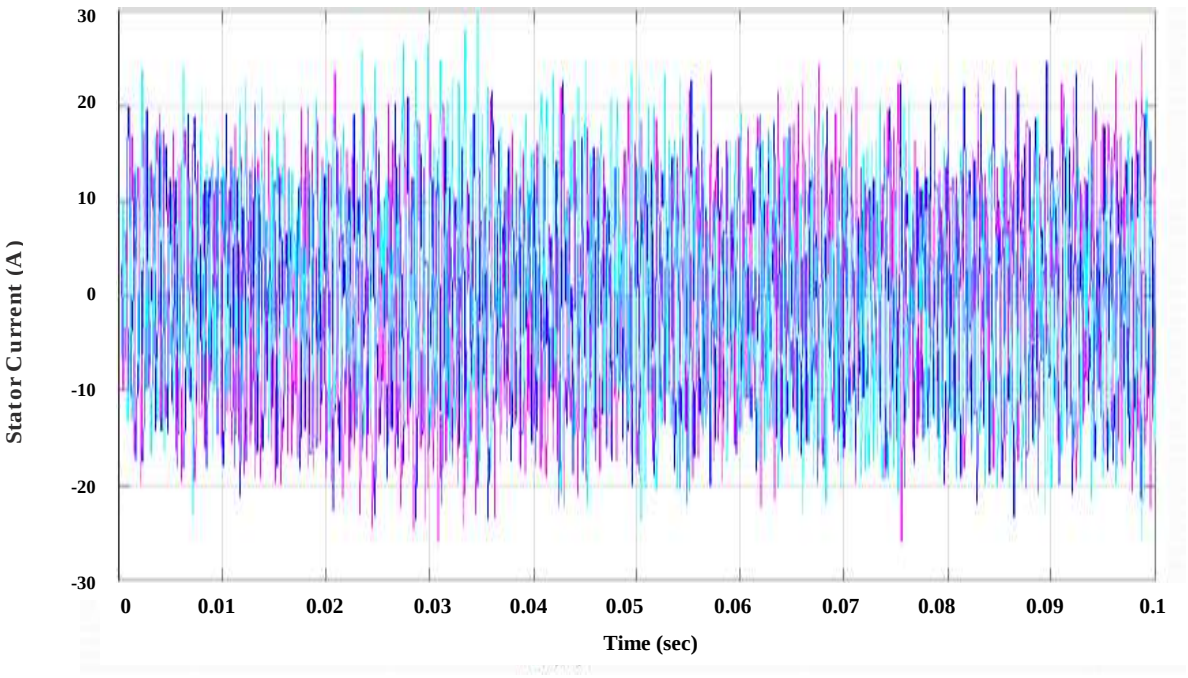


Fig.6.29 (a) : Three-phase inverter currents using FOC- CBSVPWM

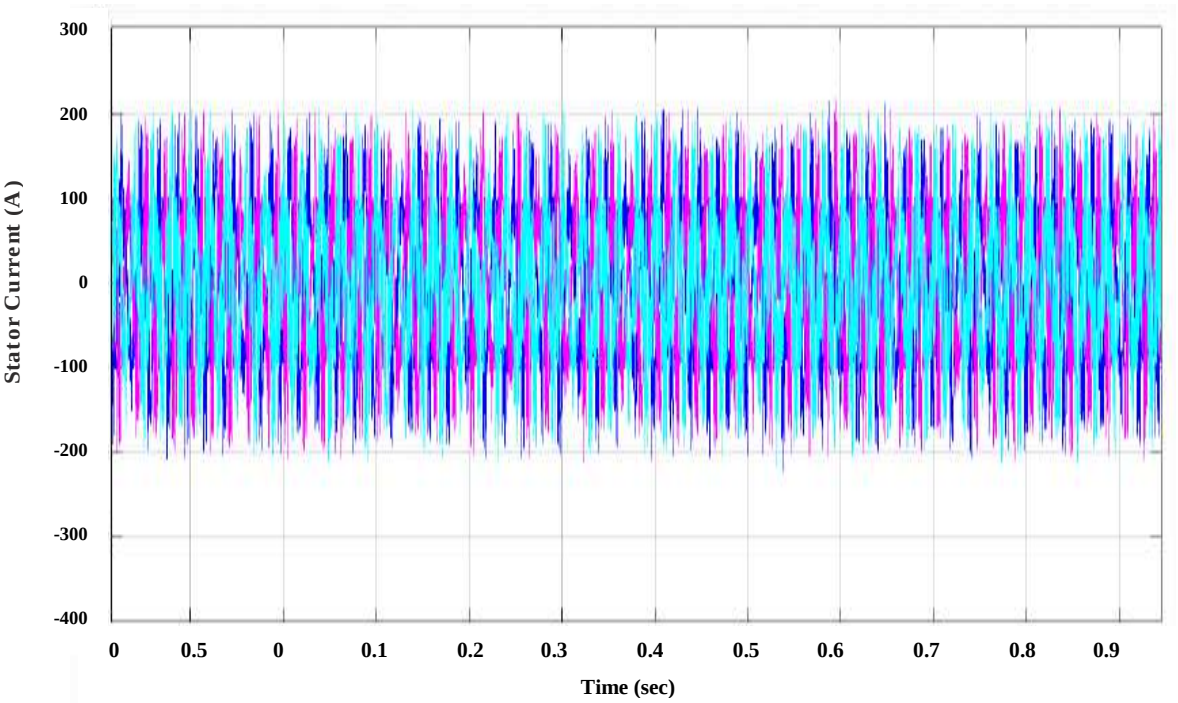


Fig.6.29 (b) : Three-phase inverter currents using DTC- CBSVPWM

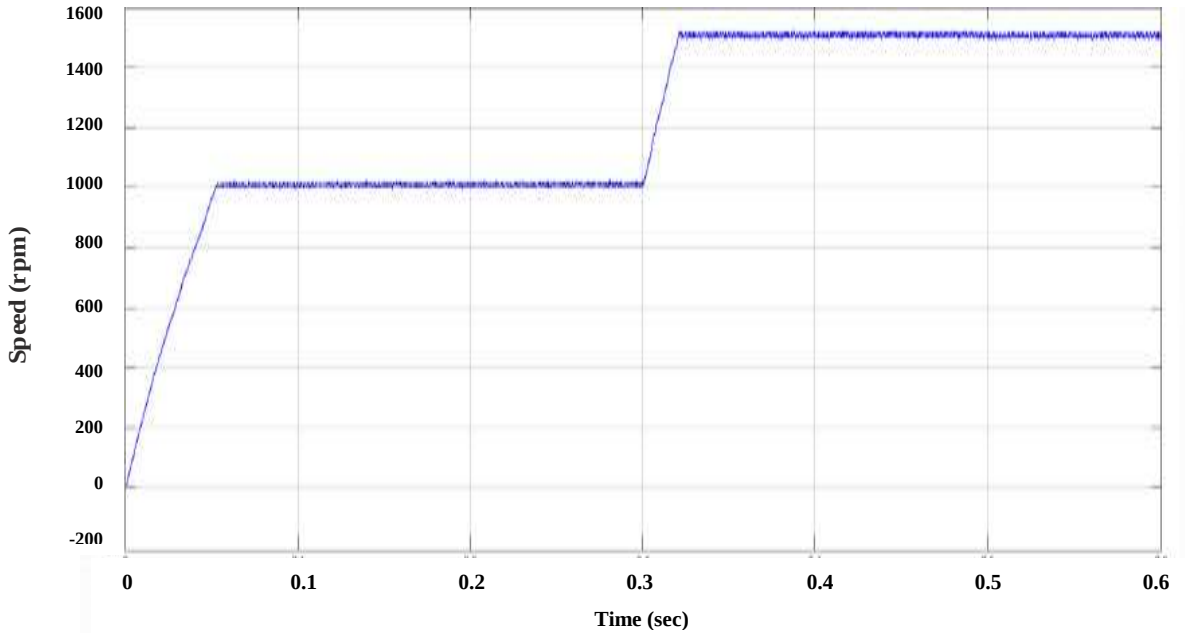


Fig. 6.30 (a) : Speed response of PMSM drive using FOC- CBSVPWM

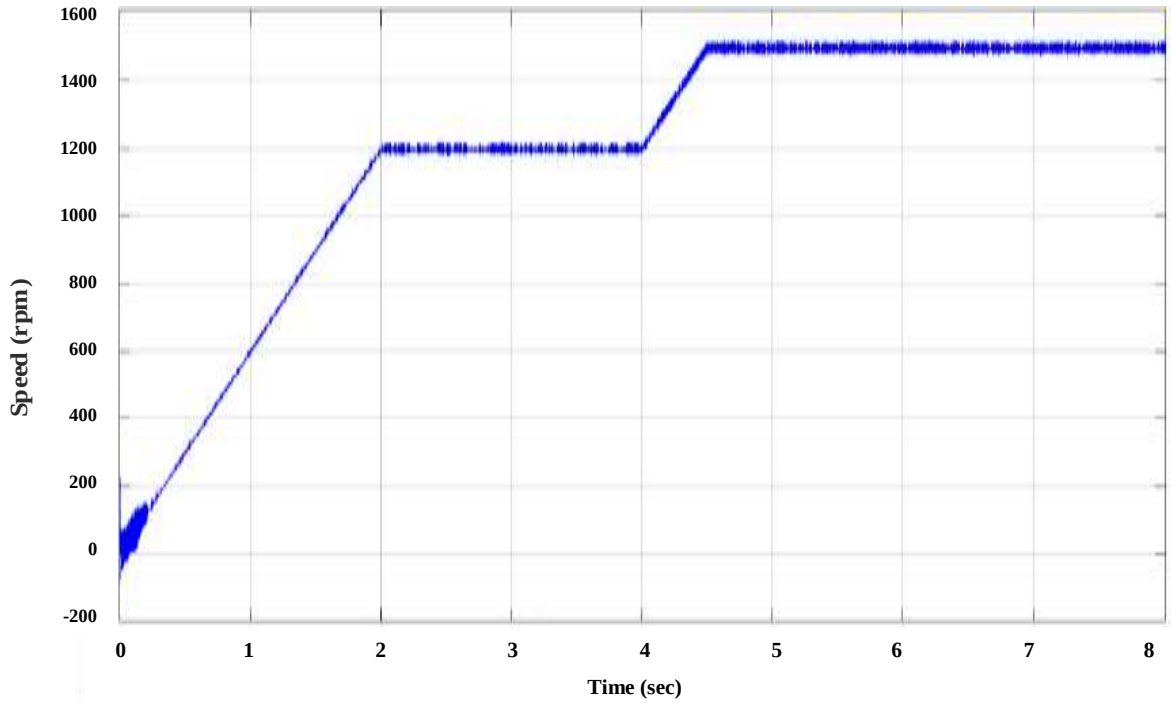


Fig.6.30 (b) : Speed response of PMSM drive using DTC- CBSVPWM

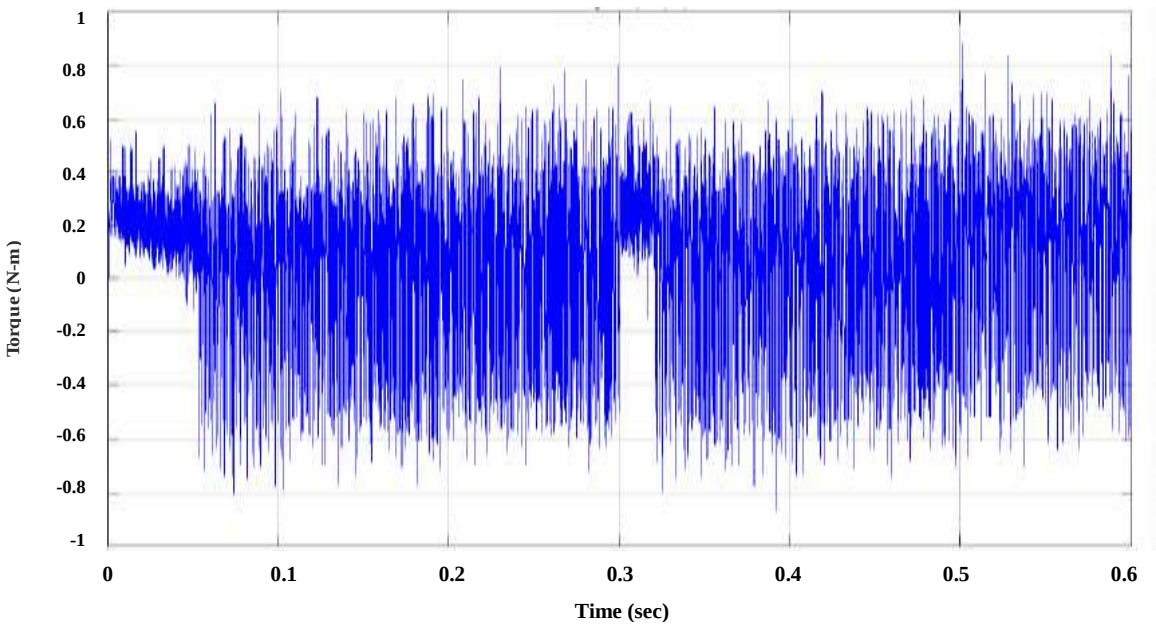


Fig.6.31 (a) : Torque response of PMSM drive using FOC- CBSVPWM

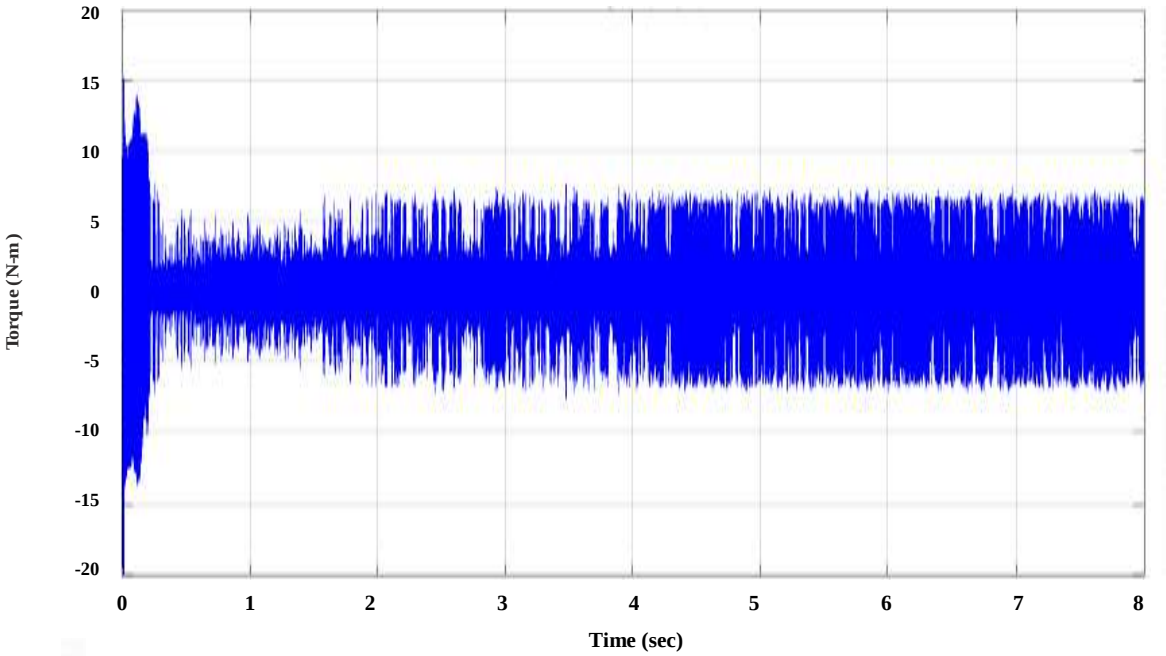


Fig.6.31 (b) : Torque response of PMSM drive using DTC- CBSVPWM

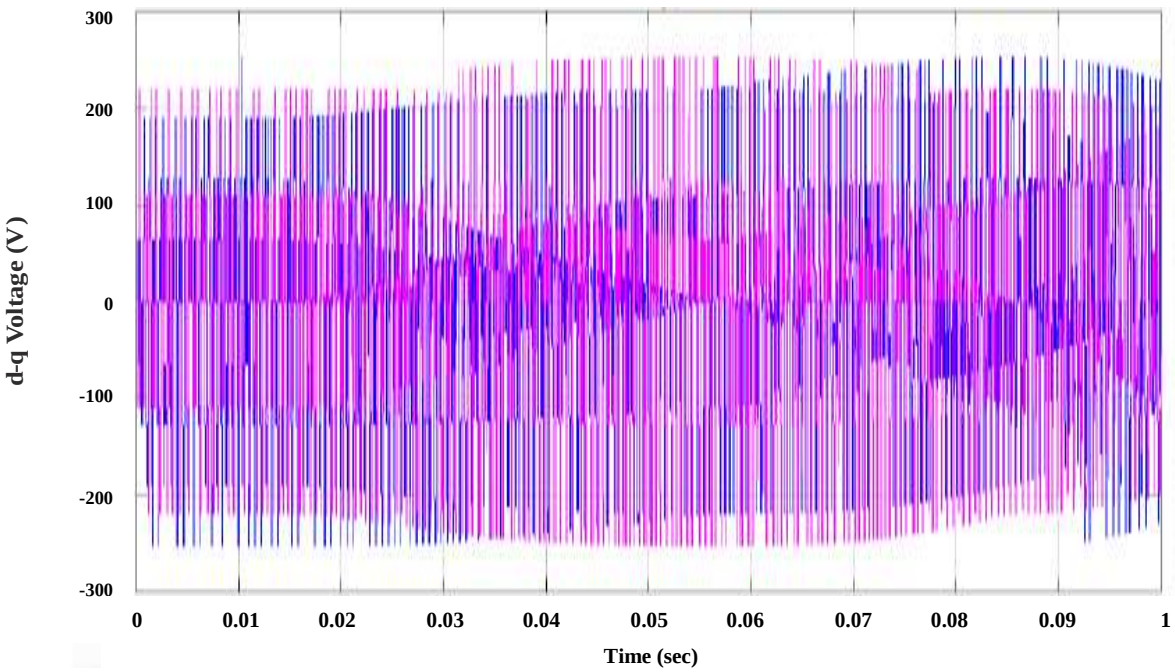


Fig.6.32 (a) : d-q voltage response of PMSM drive using FOC- CBSVPWM

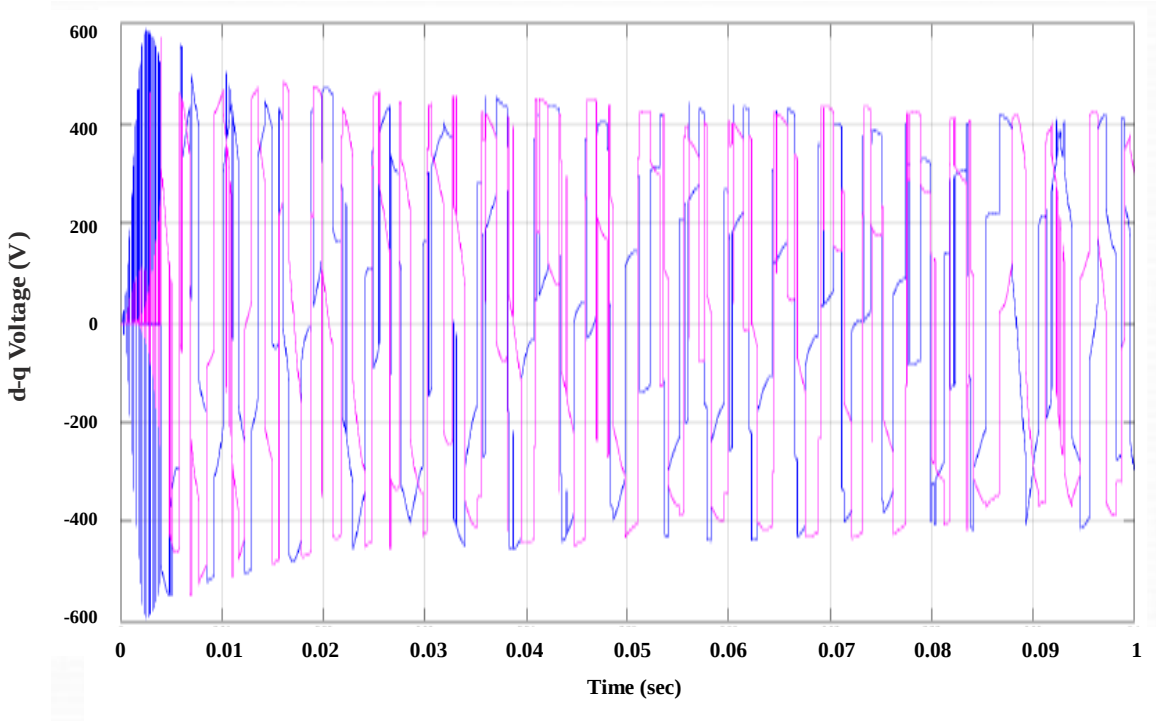


Fig.6.32 (b) : d-q voltage response of PMSM drive using DTC- CBSVPWM

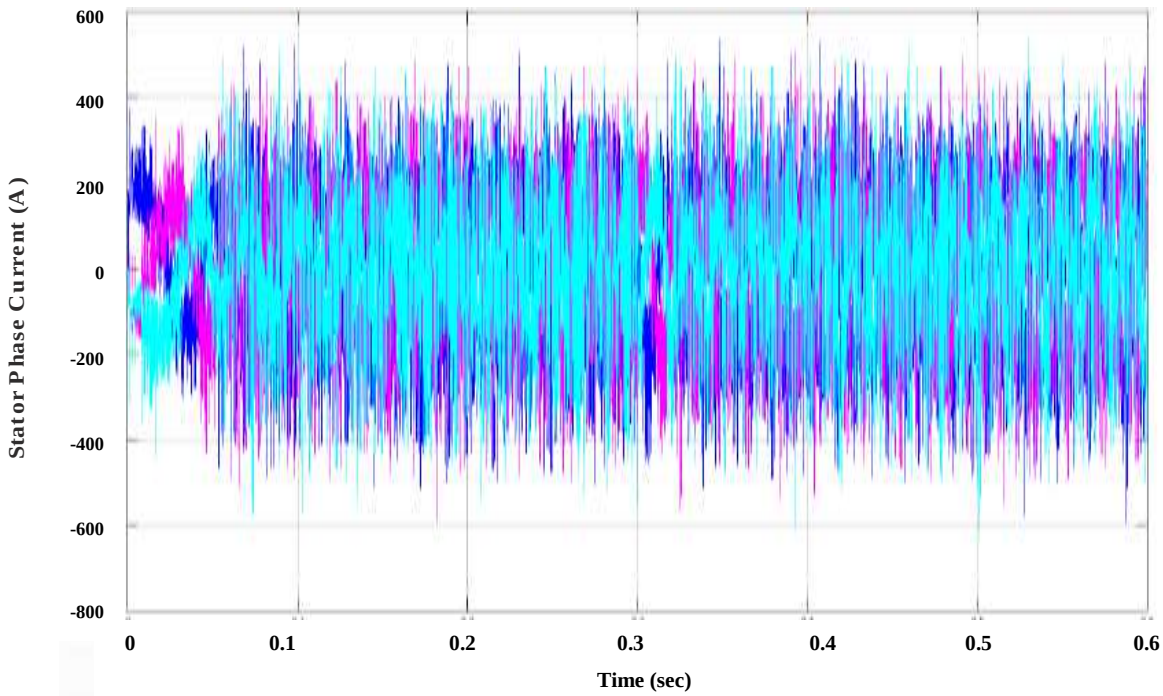


Fig.6.33 (a) : Stator current response of PMSM drive using FOC- CBSVPWM

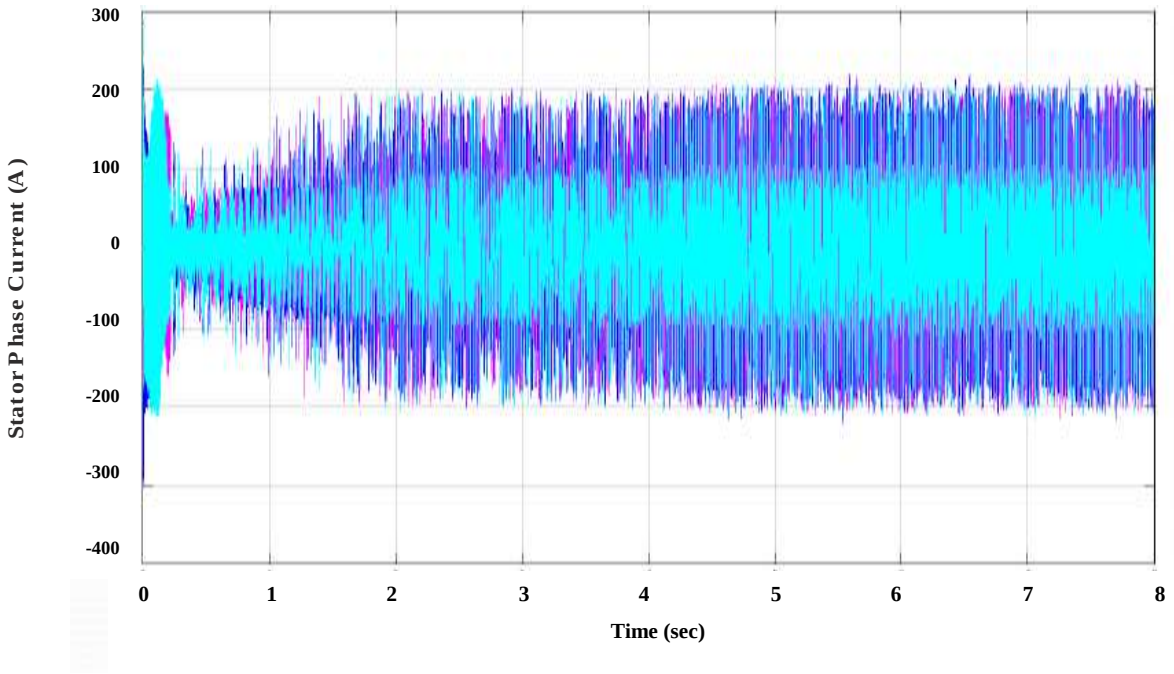


Fig.6.33 (b) : Stator current response of PMSM drive using DTC- CBSVPWM

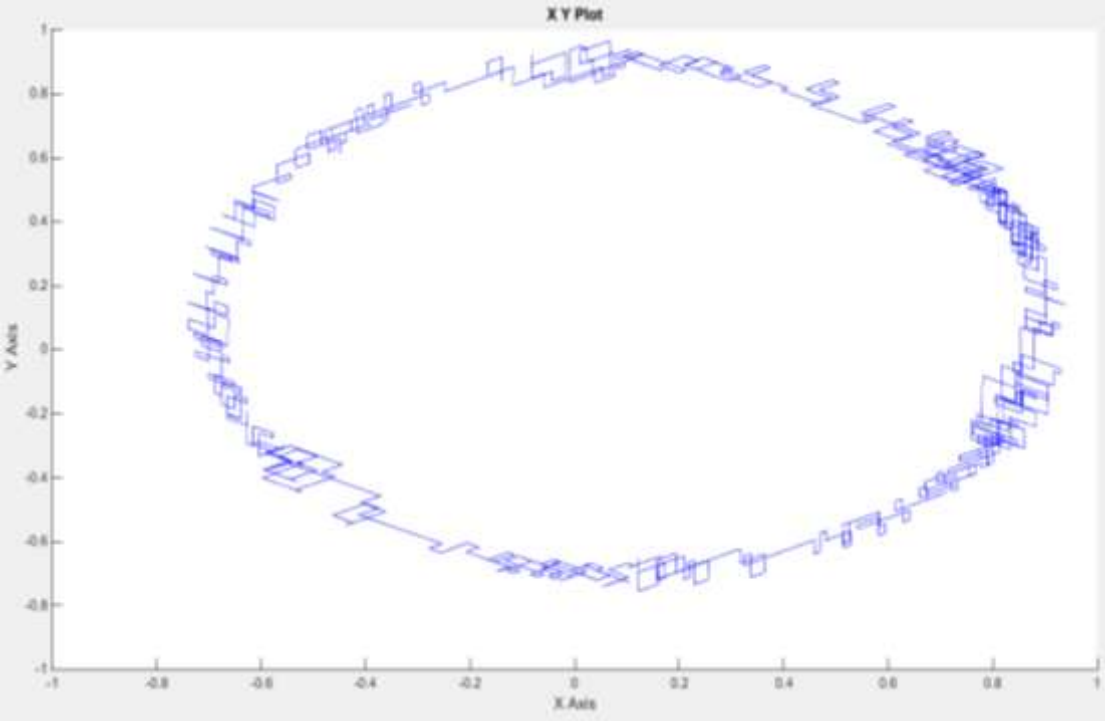


Fig. 6.34 : Stator-Rotor flux response of PMSM drive using DTC- CBSVM

From fig. 6.26 to fig 6.34 shows the performance of FOC– CBSVM with DTC-CBSVM in steady state condition Under steady state condition the reference speed value is same 1000-1500 rpm and it takes 0.05s to reach to this speed and constant up to 0.3 s. after 0.32 s it increase up to 1500 rpm and again constant. Fig.6.26 (a) &6.26(b) shows the three phase inverter line voltage waveform using FOC- CBSVM & DTC- CBSVM. Fig.6.27 (a) &6.27(b) shows the single phase inverter line voltage waveform using FOC- CBSVM & DTC- CBSVM. Fig.6.28 (a) &6.28(b) shows the single phase inverter phase voltage waveform using FOC- CBSVM & DTC- CBSVM.Fig.6.29 (a) &6.29(b) shows the three phase inverter current waveform using FOC- CBSVM & DTC- CBSVM. Fig.6.30 (a) &6.30(b) shows the Speed response using FOC- CBSVM & DTC- CBSVM. Fig.6.31 (a) &6.31(b) shows the torque response using FOC- CBSVM & DTC- CBSVM. Fig.6.32 (a) &6.32(b) shows the d-q voltage response using FOC- CBSVM & DTC- CBSVM. Fig.6.33 (a) &6.33(b) shows the Stator current response using FOC- CBSVM & DTC- CBSVM.Fig.6.34 shows the Stator-Rotor flux response using FOC- CBSVM & DTC- CBSVM.

6.9 TRANISENT PERFORMANCE OF FOC–DTC-CBSVM

6.9.1 Transient performance of FOC–DTC-CBSVM at load (3N-M)

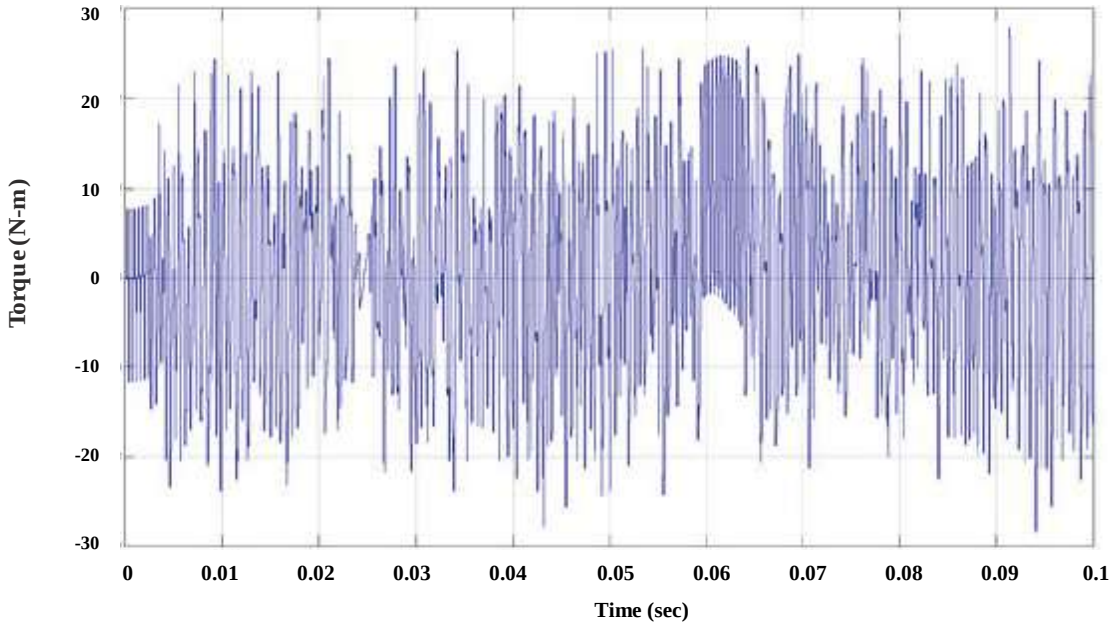


Fig.6.35 (a) : Torque response of PMSM drive using FOC- CBSVM

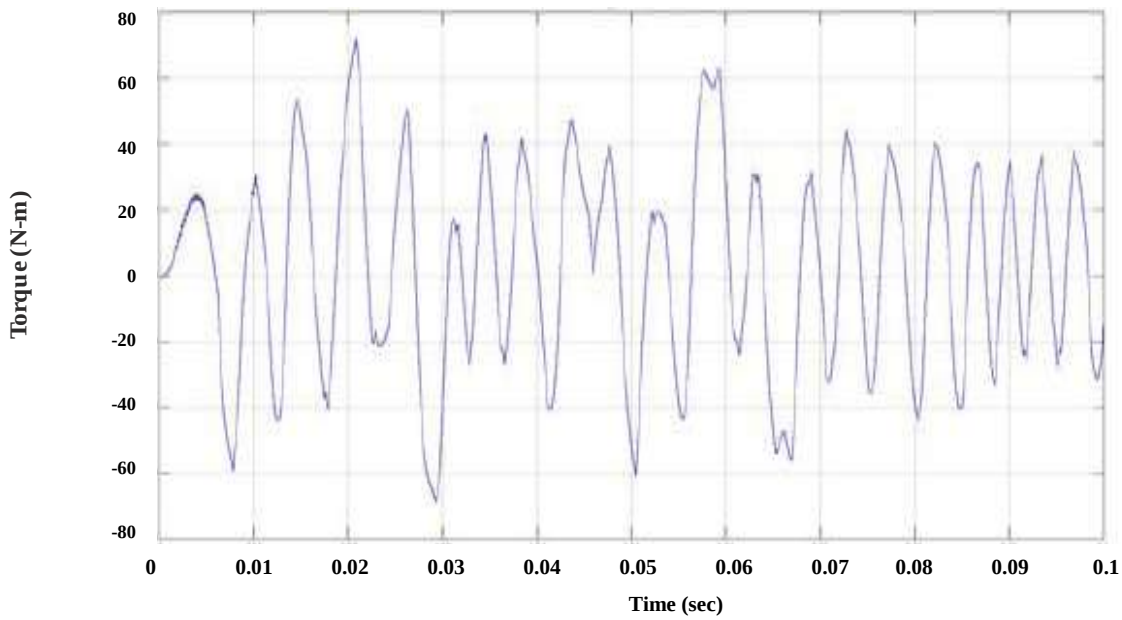


Fig.6.35 (b) : Torque response of PMSM drive using DTC- CBSVM

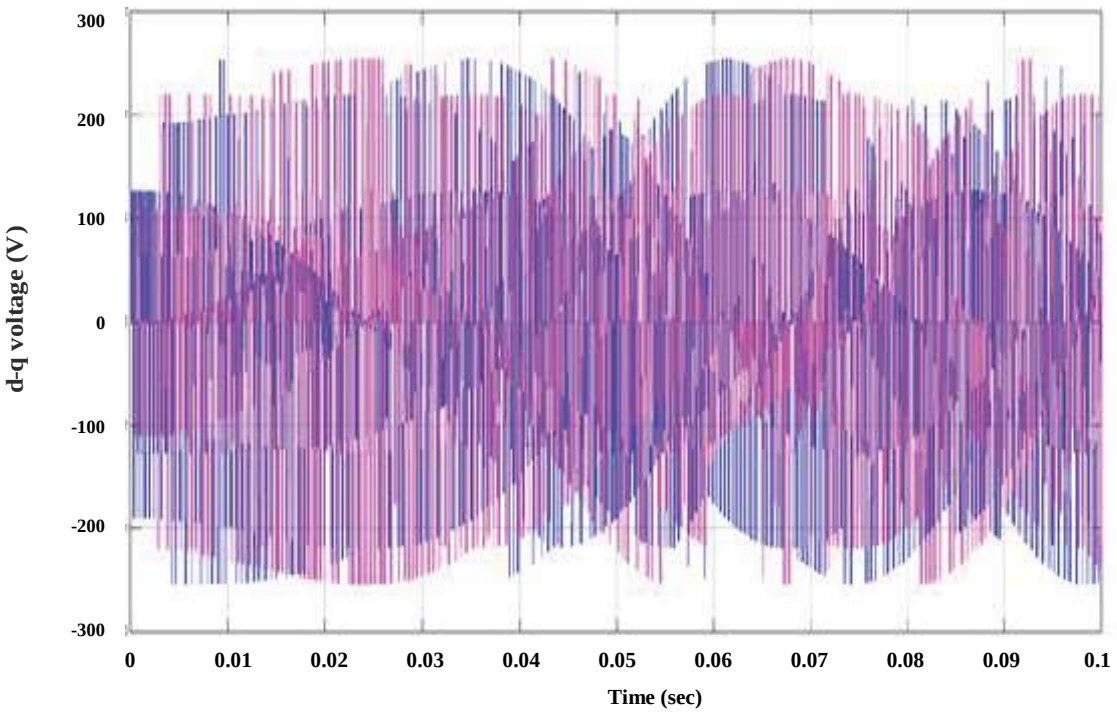


Fig.6.36 (a) : d-q voltage response of PMSM drive using FOC- CBSVM

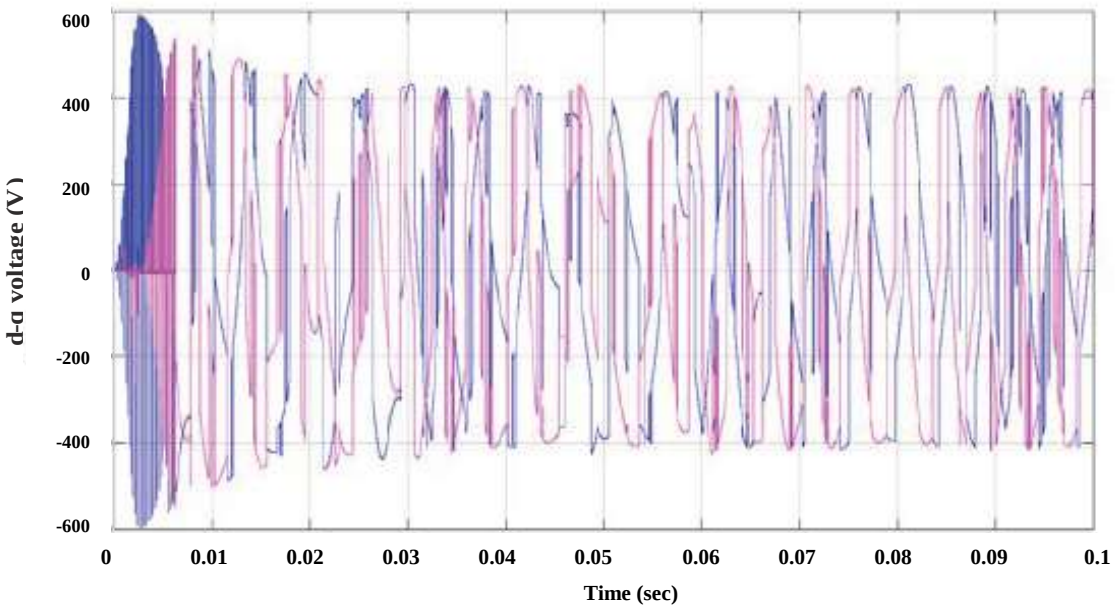


Fig.6.36 (b) : d-q voltage response of PMSM drive using DTC- CBSVM

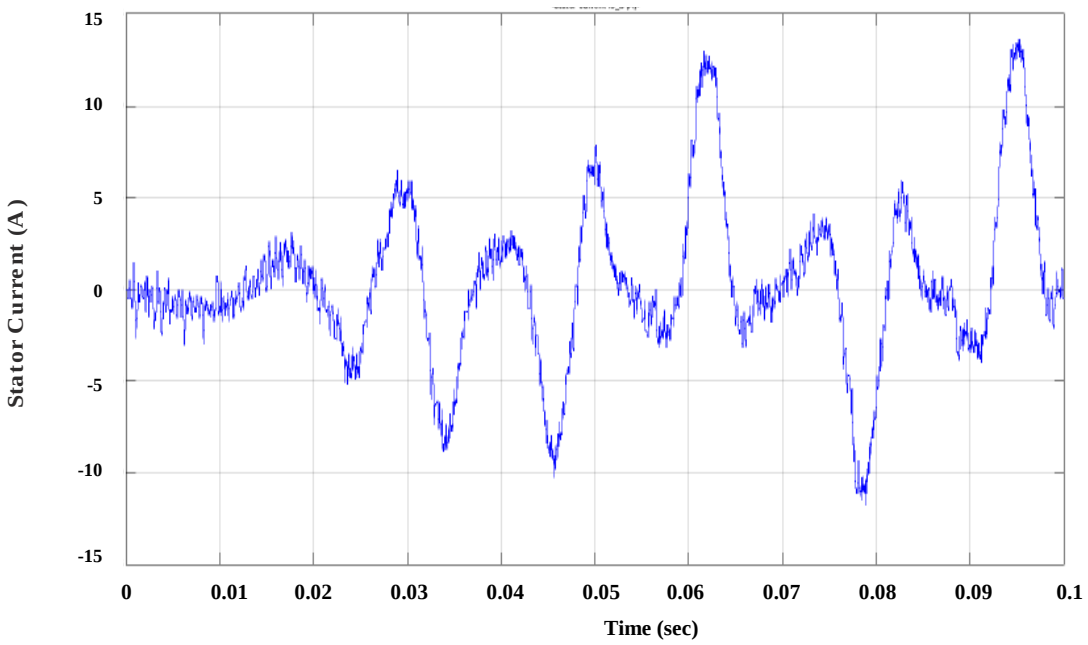


Fig.6.37 (a) : Stator current response of PMSM drive using FOC- CBSVM

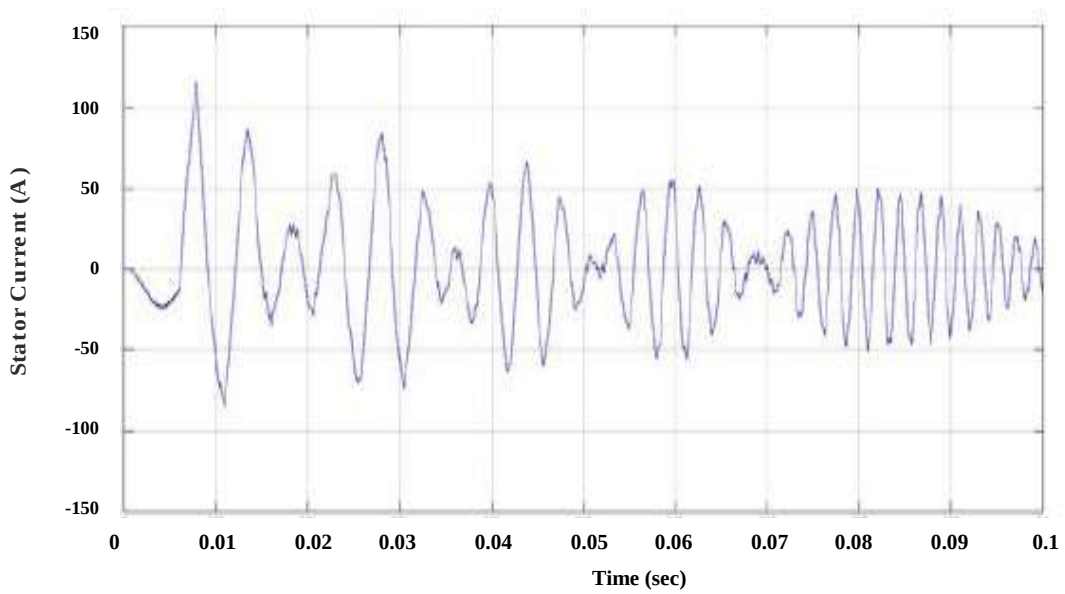


Fig.6.37 (b) : Stator current response of PMSM drive using DTC- CBSVM

6.9.2 Transient performance of FOC–DTC-CBSVM at load (5N-M)

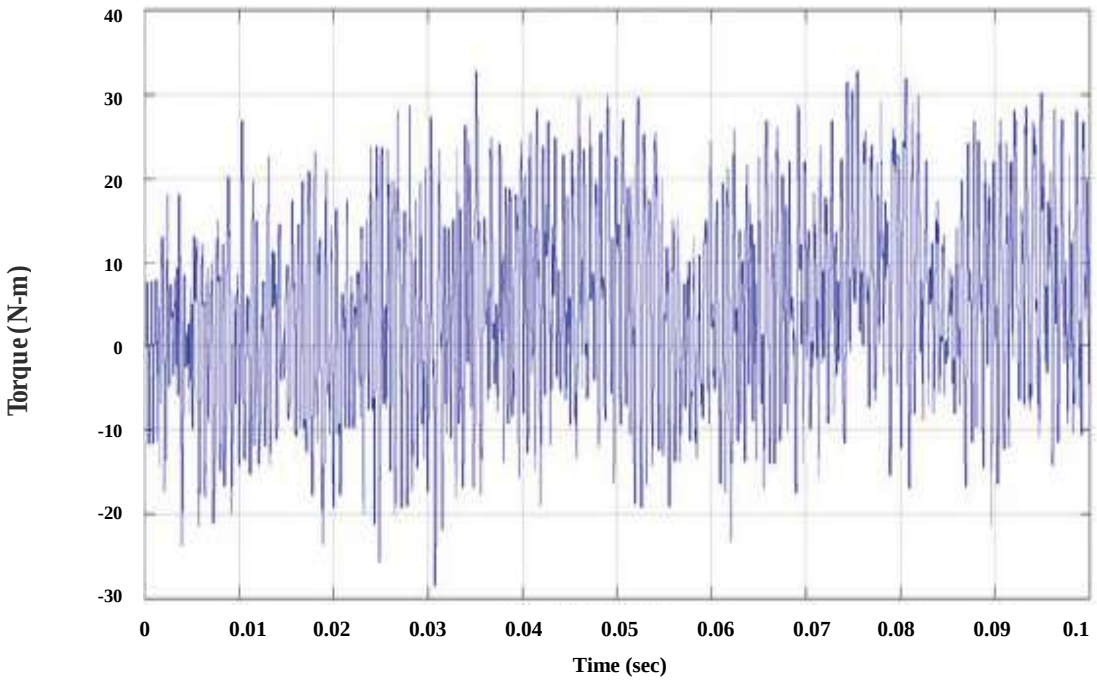


Fig.6.38 (a) : Torque response of PMSM drive using FOC- CBSVM

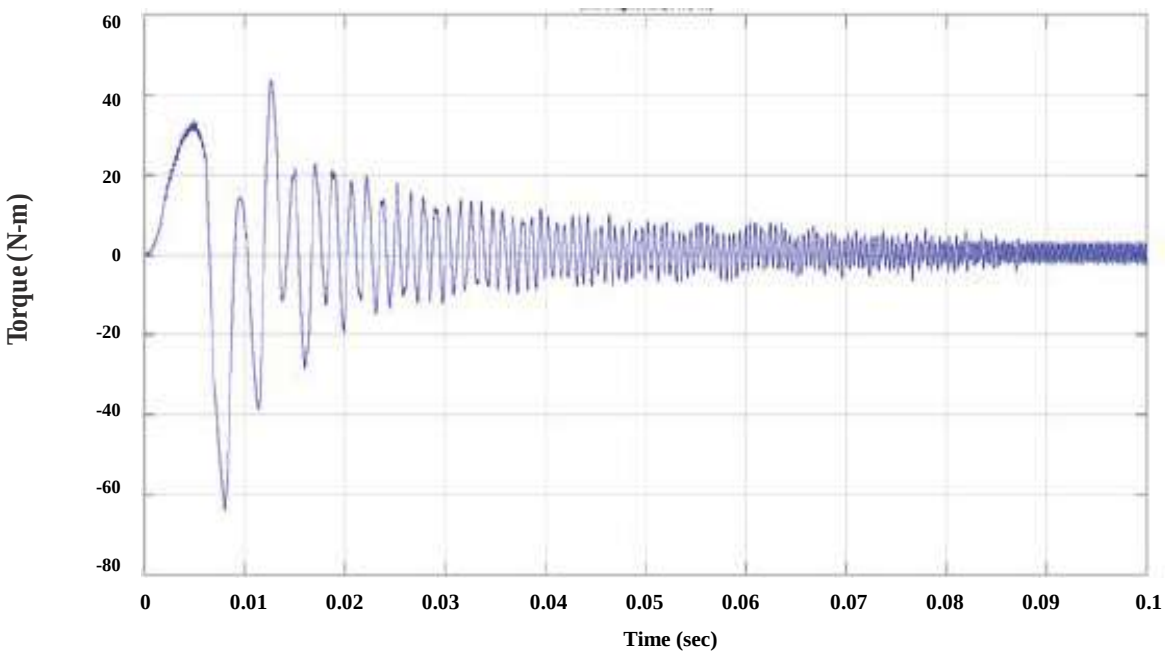


Fig.6.38 (b) : Torque response of PMSM drive using DTC- CBSVM

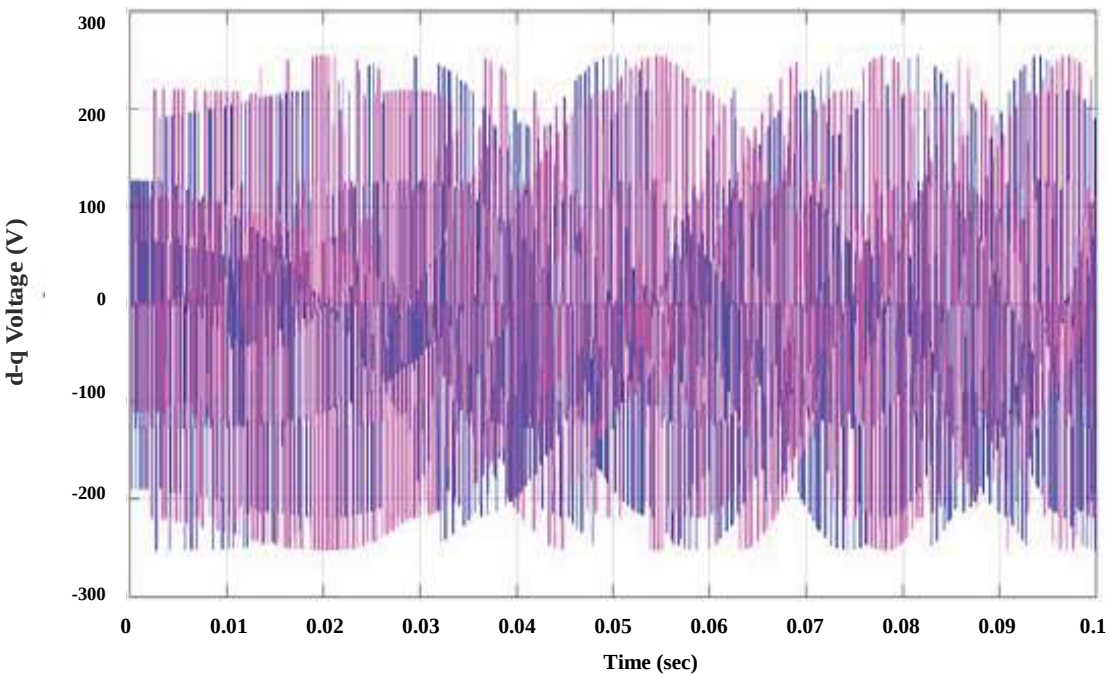


Fig.6.39 (a) : d-q voltage response of PMSM drive using FOC- CBSVM

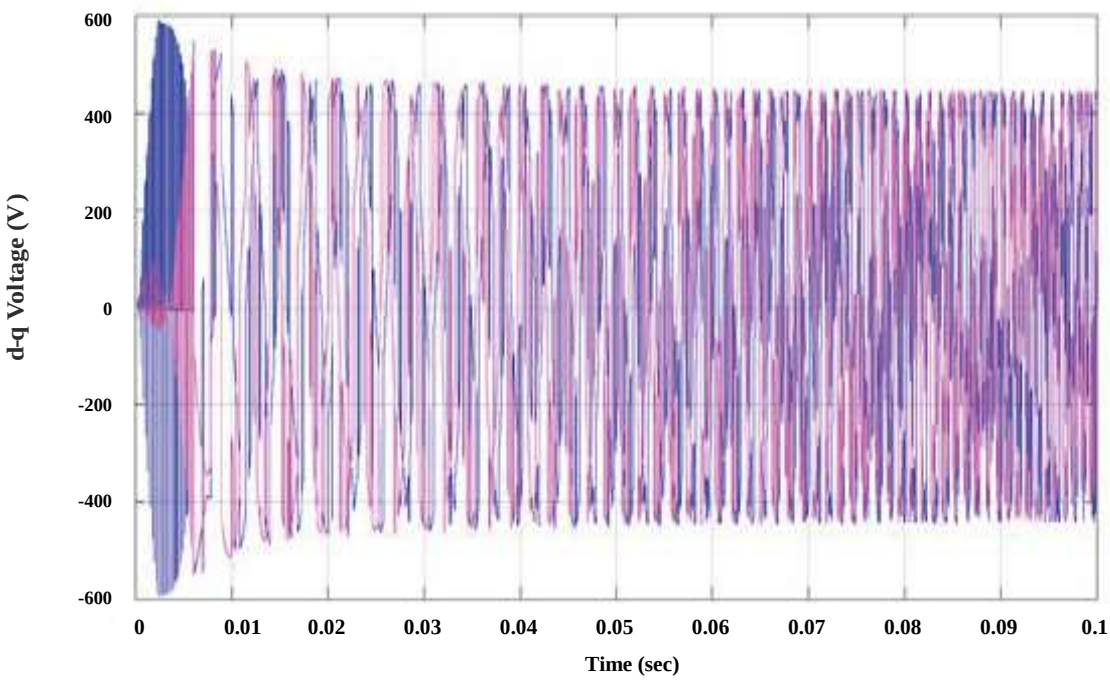


Fig.6.39 (b) : d-q voltage response of PMSM drive using DTC- CBSVM

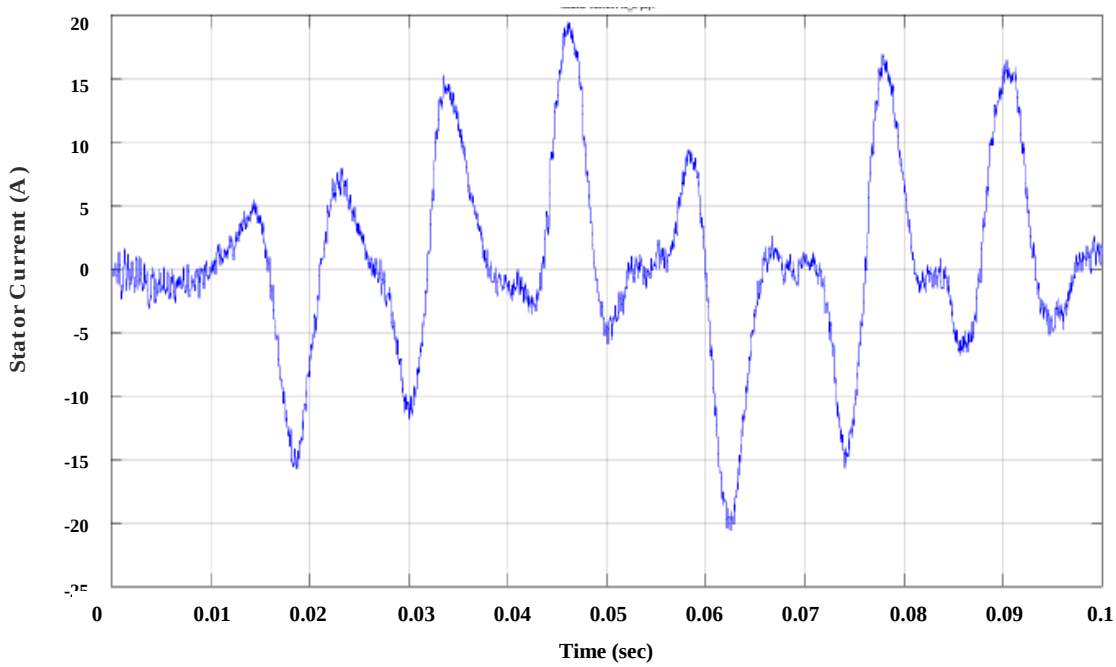


Fig.6.40 (a) : Stator current response of PMSM drive using FOC- CBSVM

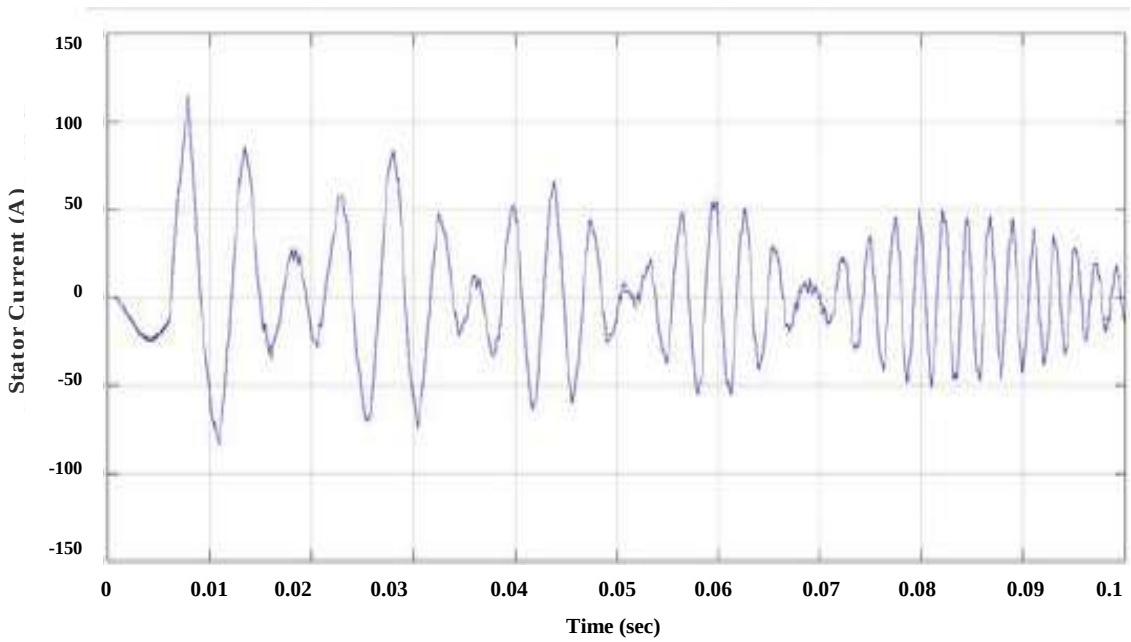


Fig.6.40 (b) : Stator current response of PMSM drive using DTC- CBSVM

6.9.3 Transient performance of FOC–DTC-CBSVM at load (10N-M)

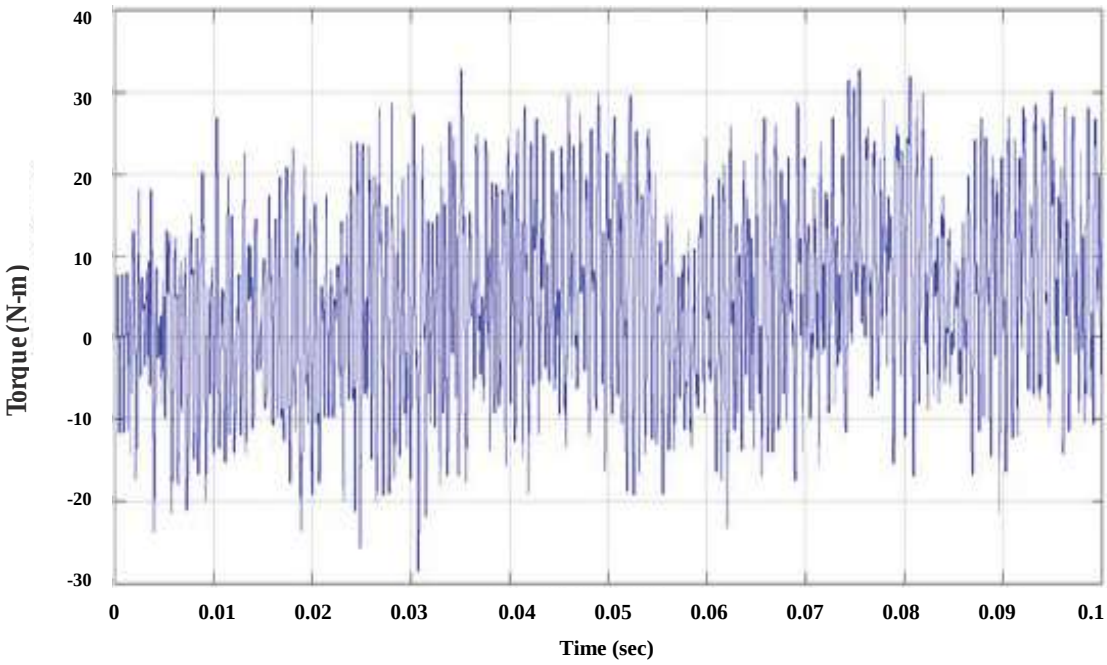


Fig.6.41 (a) : Torque response of PMSM drive using FOC- CBSVM

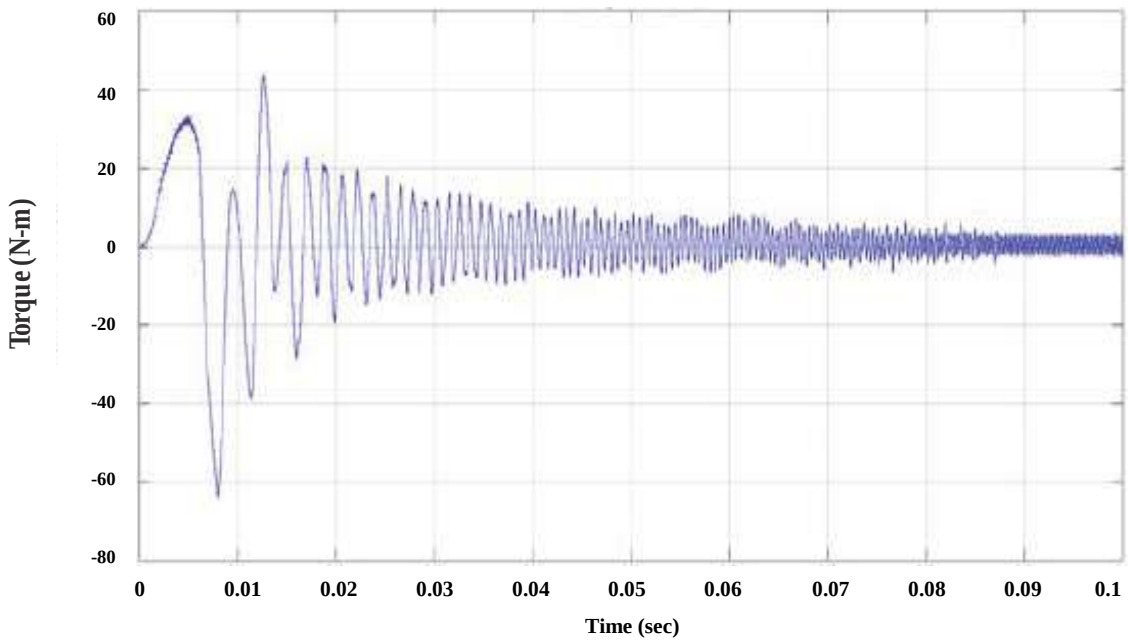


Fig.6.41 (b) : Torque response of PMSM drive using DTC- CBSVM

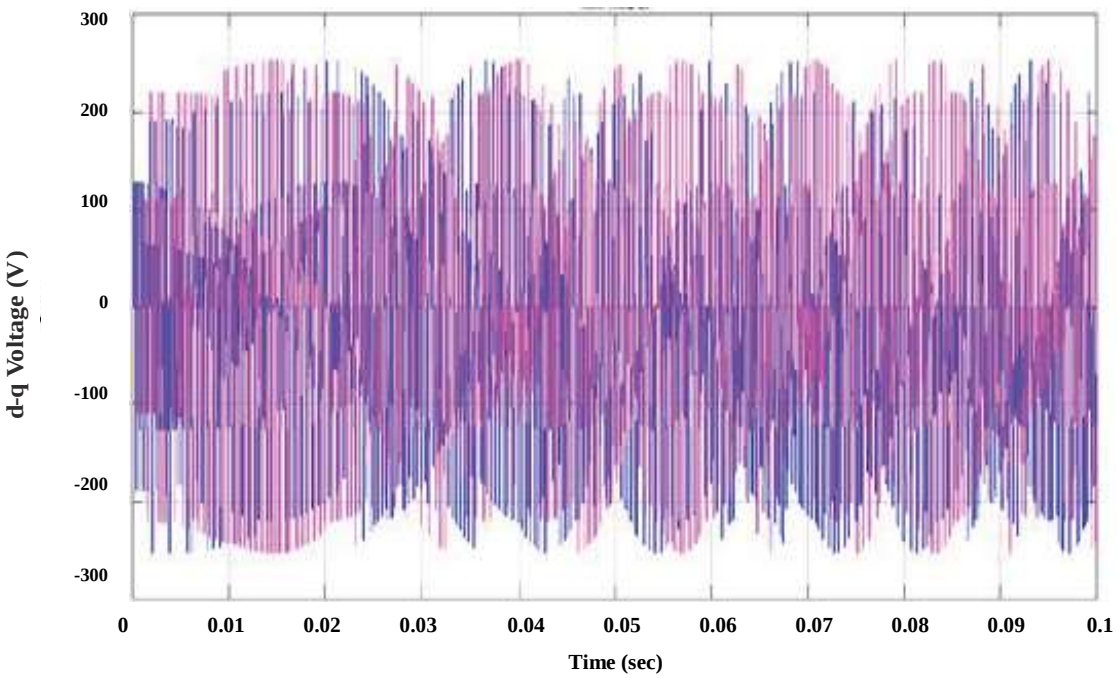


Fig.6.42 (a) : d-q voltage response of PMSM drive using FOC- CBSVM

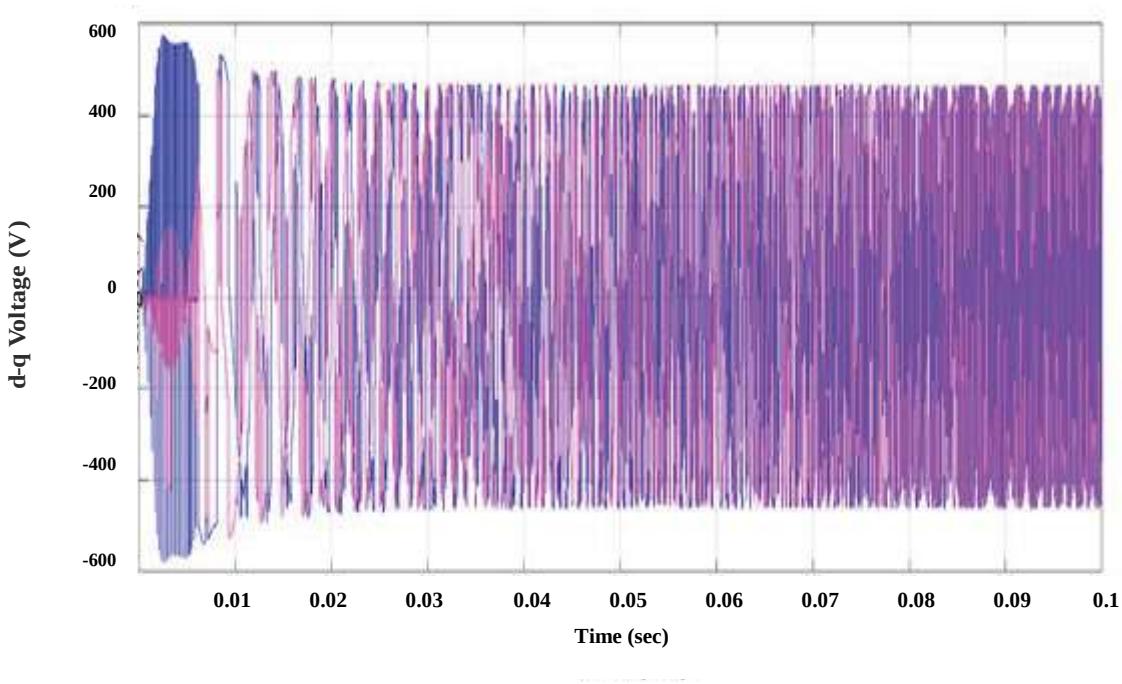


Fig.6.42 (b) : d-q voltage response of PMSM drive using DTC- CBSVM

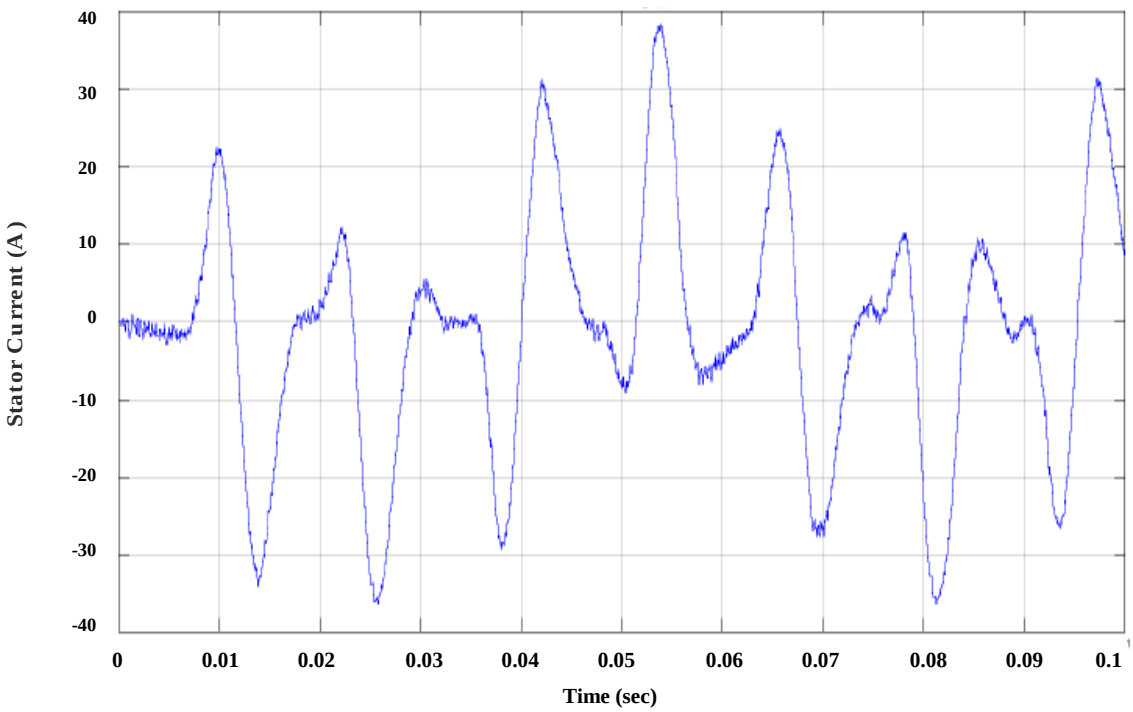


Fig.6.43 (a) : Stator current response of PMSM drive using FOC- CBSVM

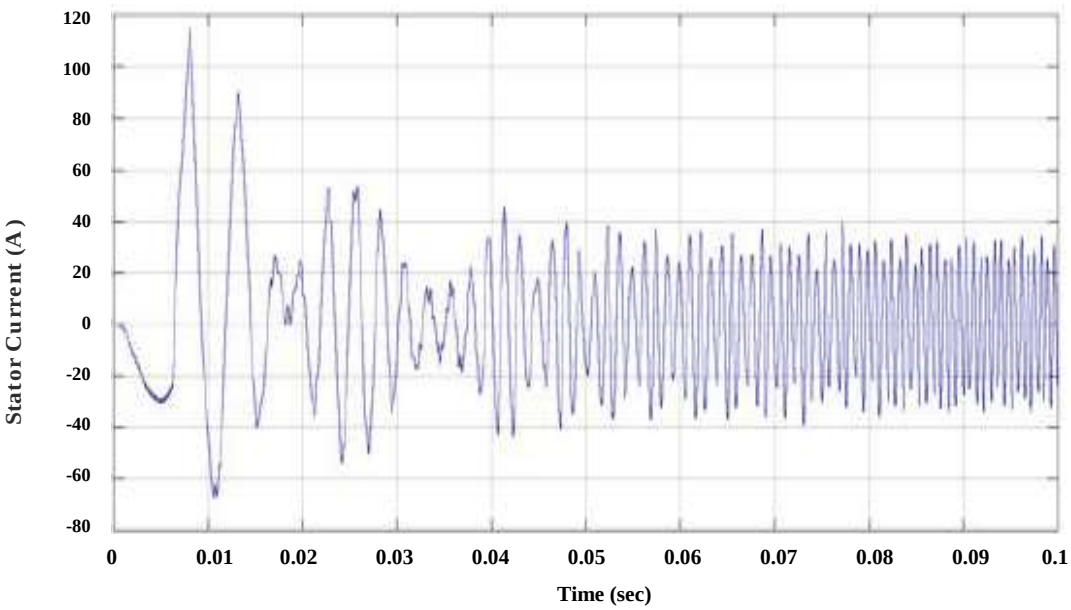


Fig.6.43 (b) : Stator current response of PMSM drive using DTC- CBSVM

6.9.4 Transient performance of FOC–DTC-CBSVM at load(15N-M)

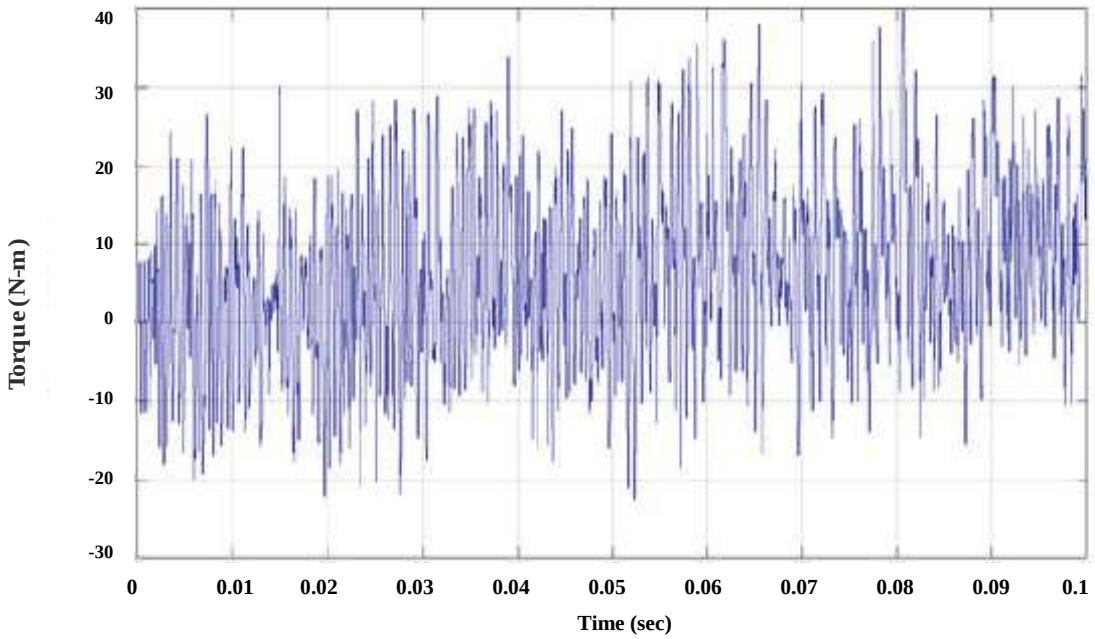


Fig.6.44 (a) : Torque response of PMSM drive using FOC- CBSVM

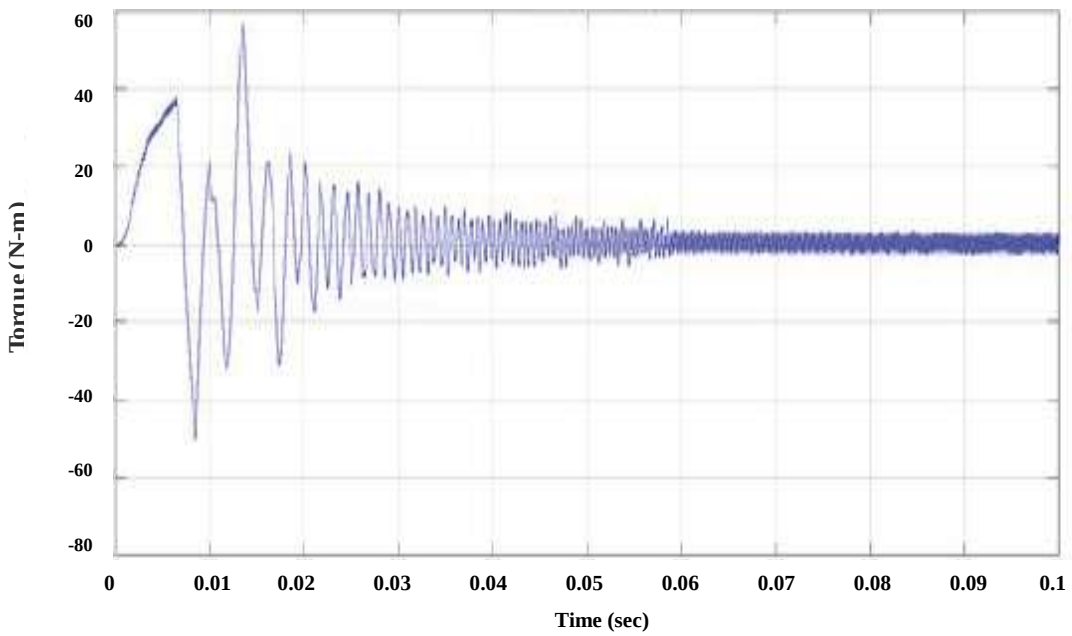


Fig.6.44 (b) : Torque response of PMSM drive using DTC- CBSVM

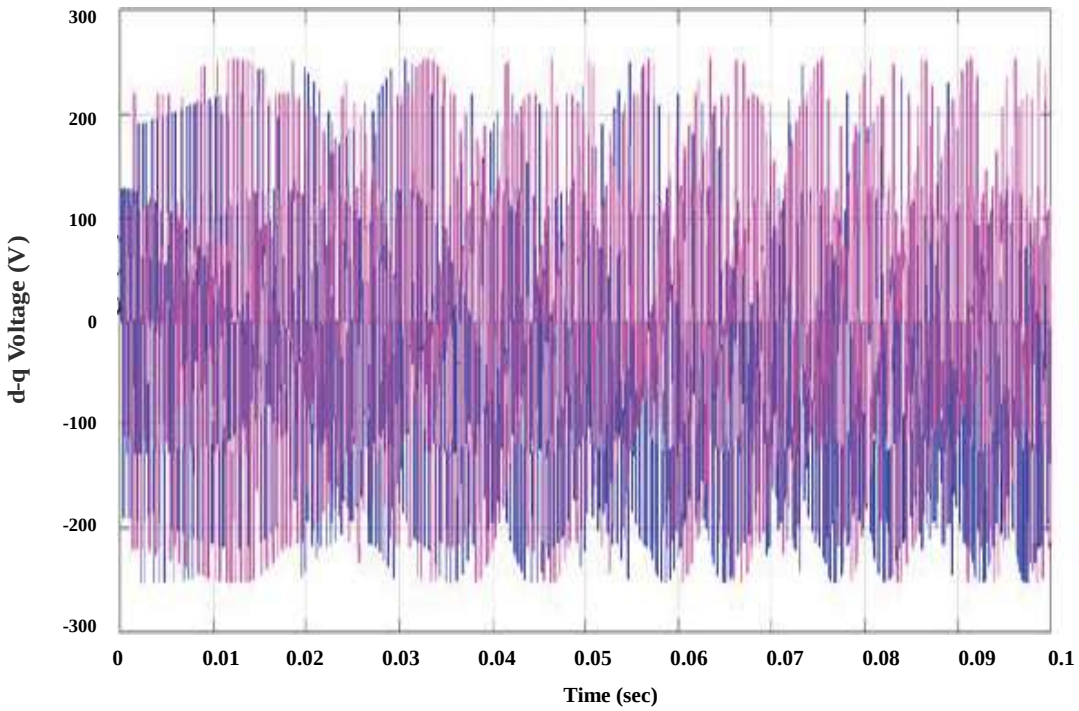


Fig.6.45 (a) : d-q voltage response of PMSM drive using FOC- CBSVM

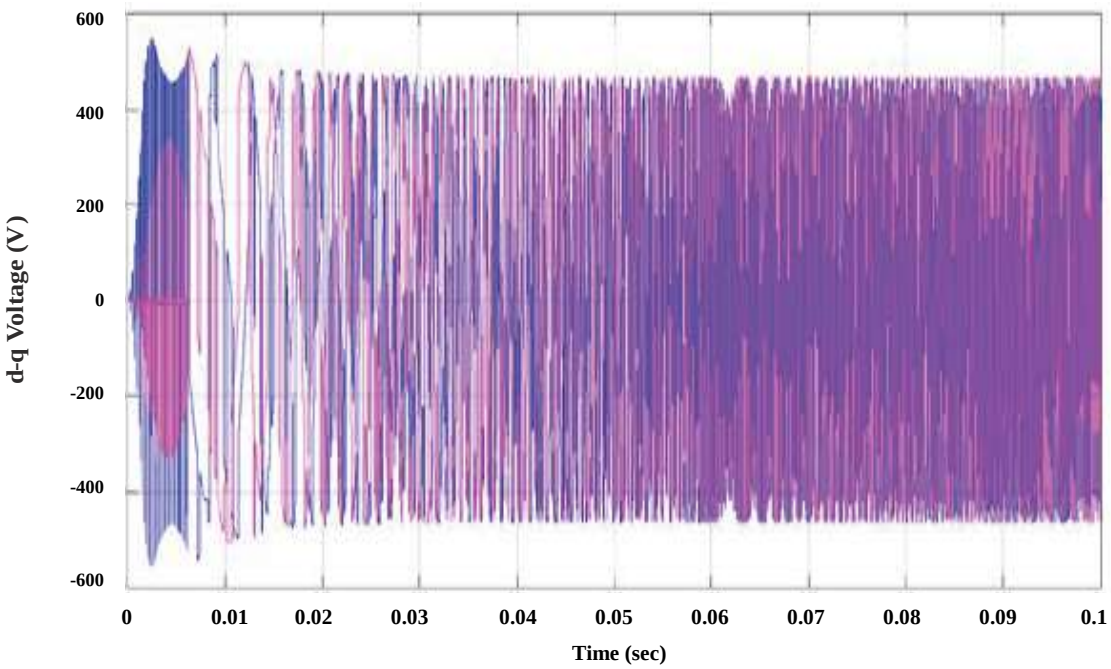


Fig.6.45 (b) : d-q voltage response of PMSM drive using DTC- CBSVM

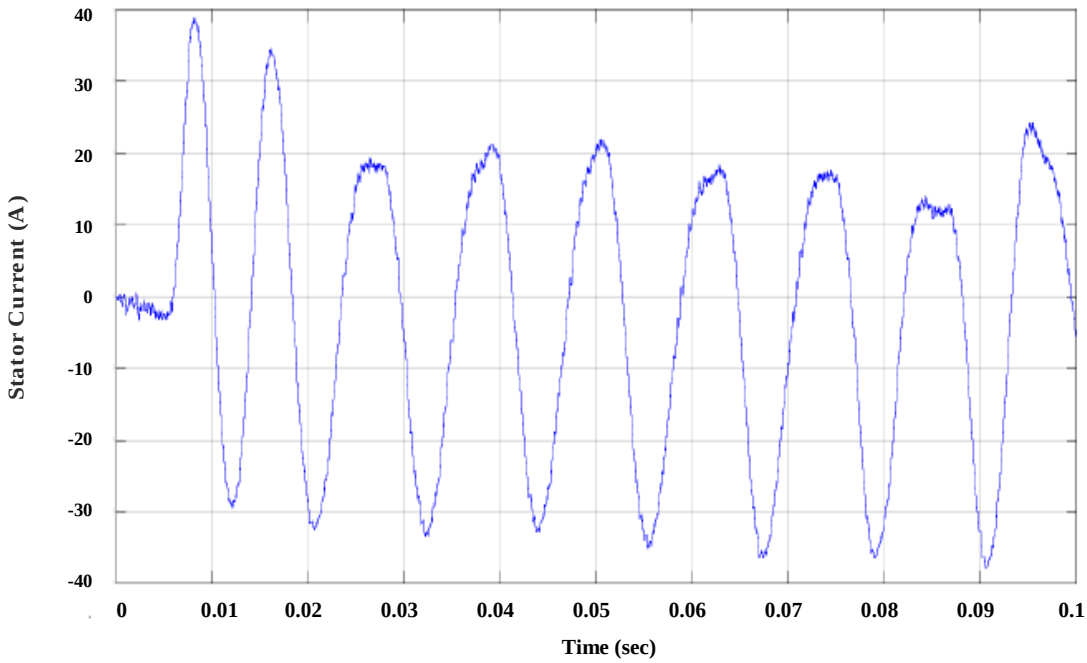


Fig.6.46 (a) : Stator current response of PMSM drive using FOC- CBSVM

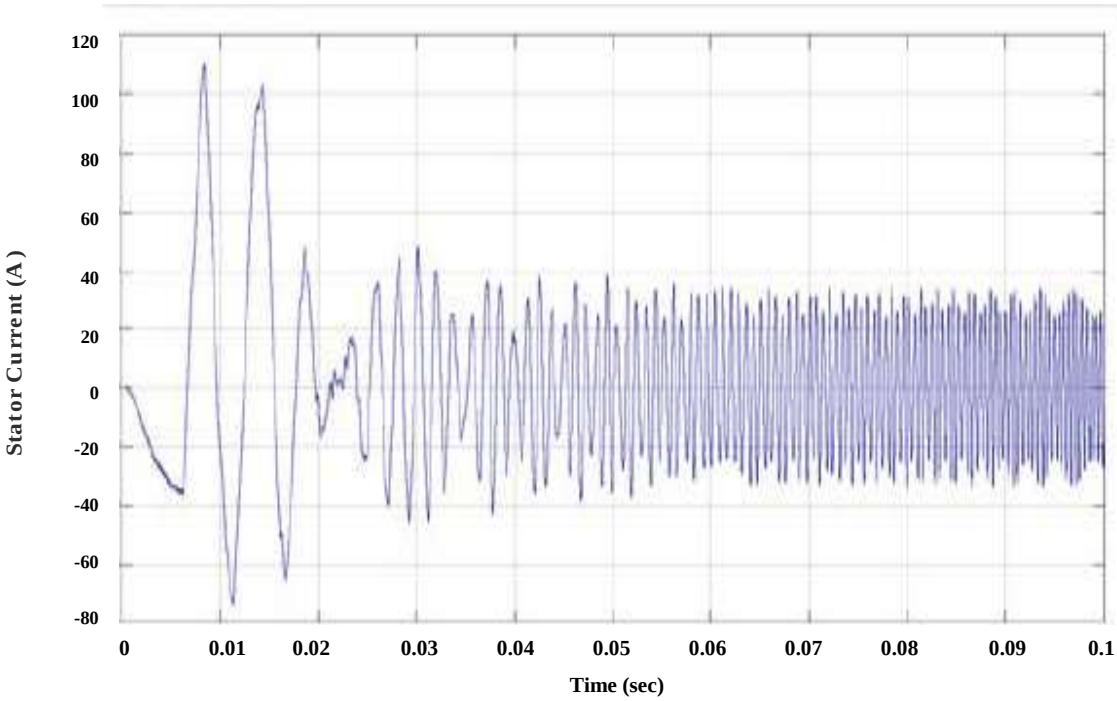


Fig.6.46 (b) : Stator current response of PMSM drive using DTC- CBSVM

From fig. 6.35to fig 6.46 shows the performance of FOC– CBSVM with DTC-CBSVM in tranisent condition at 3N-m,5N-m, 10N-m &15N-m respectively. At 3 N.m, Fig.6.35 (a) &6.35(b) shows the torque response using FOC- CBSVM & DTC-CBSVM. Fig.6.36 (a) &6.36(b) shows the d-q voltage response using FOC- CBSVM & DTC- CBSVM. Fig.6.37 (a) &6.37(b) shows the Stator current response using FOC- CBSVM & DTC- CBSVM.At 5 N.m, Fig.6.38 (a) &6.38(b) shows the torque response using FOC- CBSVM & DTC- CBSVM. Fig.6.39 (a) &6.39(b) shows the d-q voltage response using FOC- CBSVM & DTC- CBSVM. Fig.6.40 (a) &6.40(b) shows the Stator current response using FOC- CBSVM & DTC- CBSVM. At 10 N.m, Fig.6.41 (a) &6.41(b) shows the torque response using FOC- CBSVM & DTC-CBSVM. Fig.6.42 (a) &6.42(b) shows the d-q voltage response using FOC- CBSVM & DTC- CBSVM. Fig.6.43 (a) &6.43(b) shows the Stator current response using FOC- CBSVM & DTC- CBSVM.At 15 N.m, Fig.6.44 (a) &6.44(b) shows the torque response using FOC- CBSVM & DTC- CBSVM. Fig.6.45 (a) &6.45(b) shows the d-q voltage response using FOC- CBSVM & DTC- CBSVM. Fig.6.46 (a) &6.465 (b) shows the Stator current response using FOC- CBSVM & DTC- CBSVM.

6.8 THD ANALYSIS OF LINE VOLTAGE AND CURRENT OF THREE LEVEL DIODE CLAMPED INVERTER

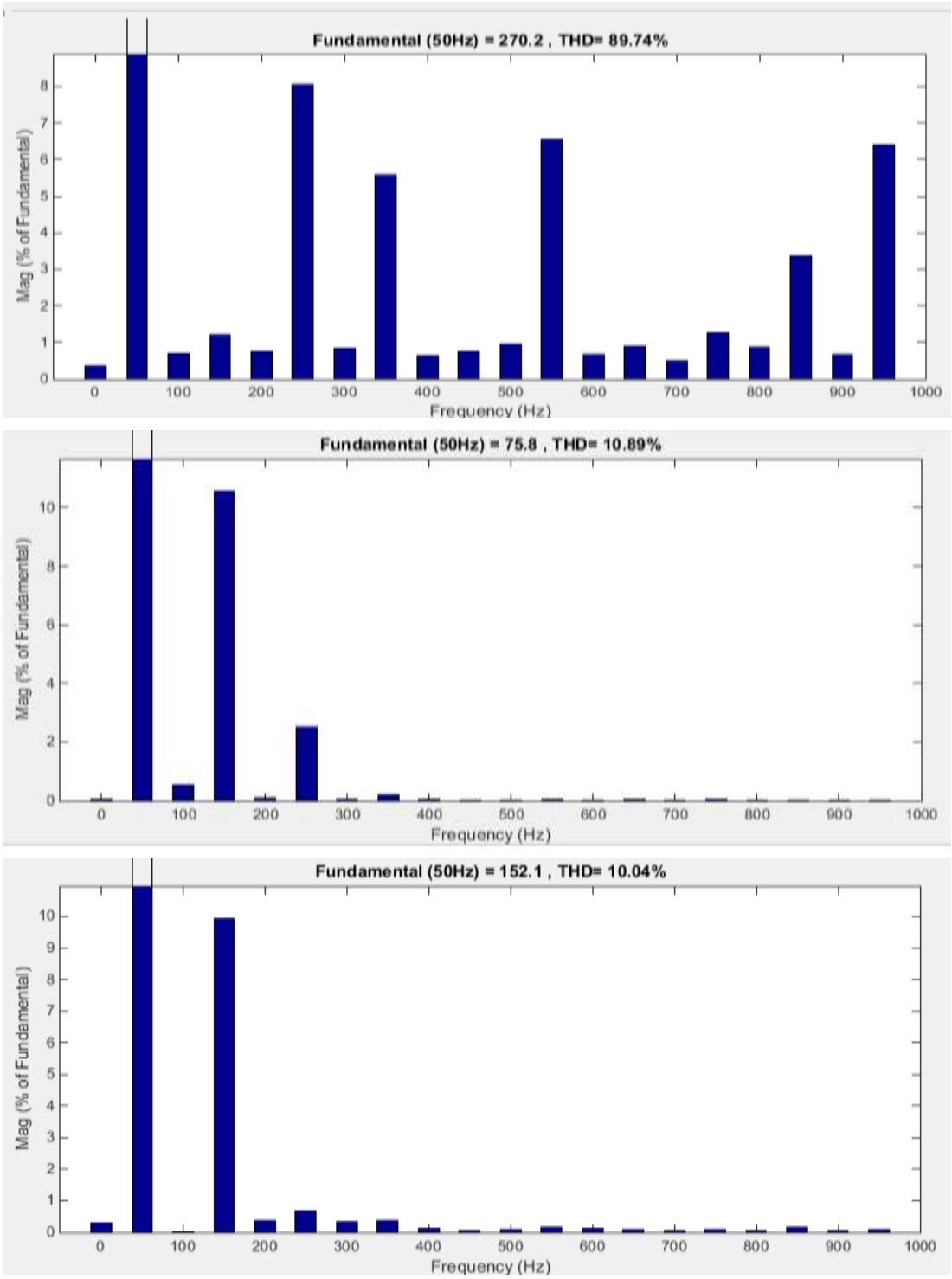


Fig. 6.47 : THD of line voltage (a) PWM (b) SVPWM (c) CBSVPWM using FOC

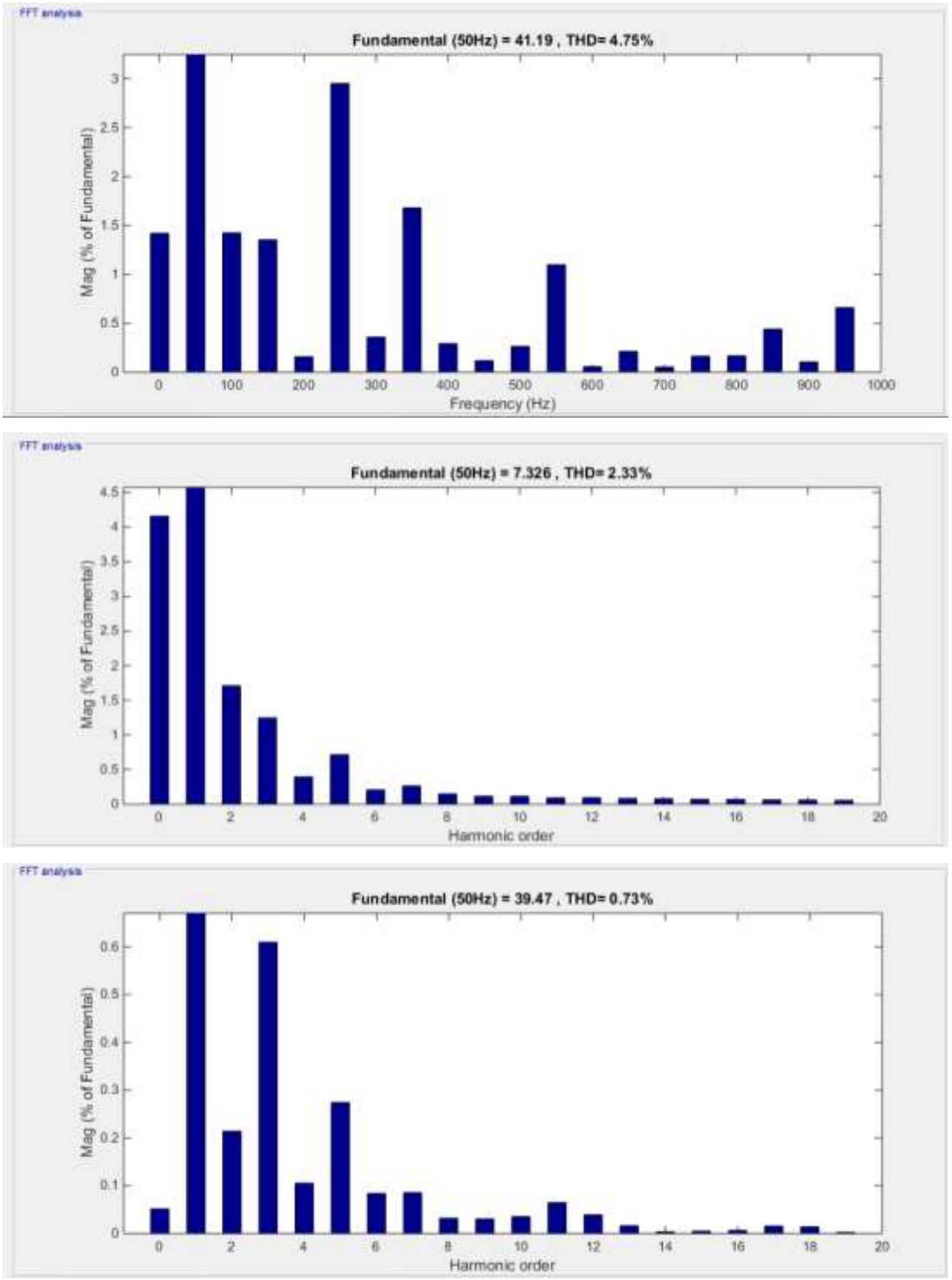


Fig.6.48 : THD of line current (a) PWM (b) SVPWM (c) CBSVPWM using FOC

Table. 6.3 : Specification of PMSM for three level inverter

Sr. No.	PMSM Parameter	Value
1.	Stator Resistance Rs	1.6 Ω
2.	d-axis Inductance Ld	0.006366H
3.	q-axis Inductance Lq	0.006366H
4.	Permanent Magnet Flux	0.1862Wb
6.	No of Pole pairs	2
6.	Movement of Inertia(J)	0.0001864 Kg/m^2
7.	Viscous coefficient(f)	0.00006396 Nms

Table 6.4 : THD analysis of three level DCMLI using PWM, SVM, and CBSVM

THD	PWM	SVPWM	CBSVPWM
Line Voltage	89.74%	10.89%	10.04%
Line Current	4.75%	2.33%	0.73%

Table 6.5 : Torque ripple analysis of FOC-CBSVM and DTC-CBSVM based three level DCMLI fed PMSM drive

% Torque Ripples	FOC-PWM	FOC-SVPWM	FOC-CBSVM	DTC-CBSVM
	20%	18%	15.38%	**10.52 %**

Fig. 6.47 & Fig.6.48 shows THD analysis of line voltage & current of FOC based three level diode clamped inverter using PWM, SVPWM and CBSVPWM. Table 6.4. Shows THD analysis of FOC based three level diode clamped inverter using PWM, SVPWM, CBSVPWM. Table 6.5 shows torque ripple analysis of FOC-CBSVM and DTC-CBSVM based three level DCMLI fed PMSM drive.

6.11 ANALYSIS OF FOC-CB FED PMSM DRIVE AT DIFFERENT INVERTER SWITCHING FREQUENCIES

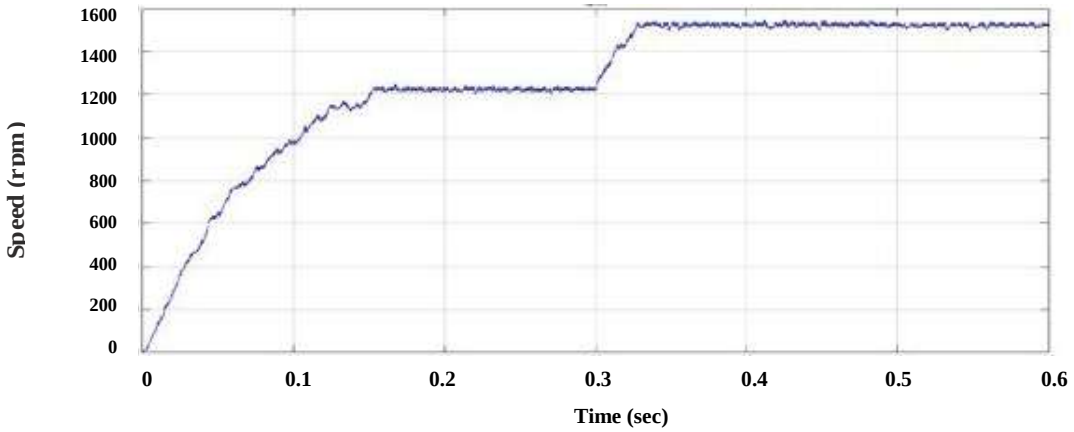


Fig.6.49 (a) : Output speed response using FOC-CB using 2.5KHz

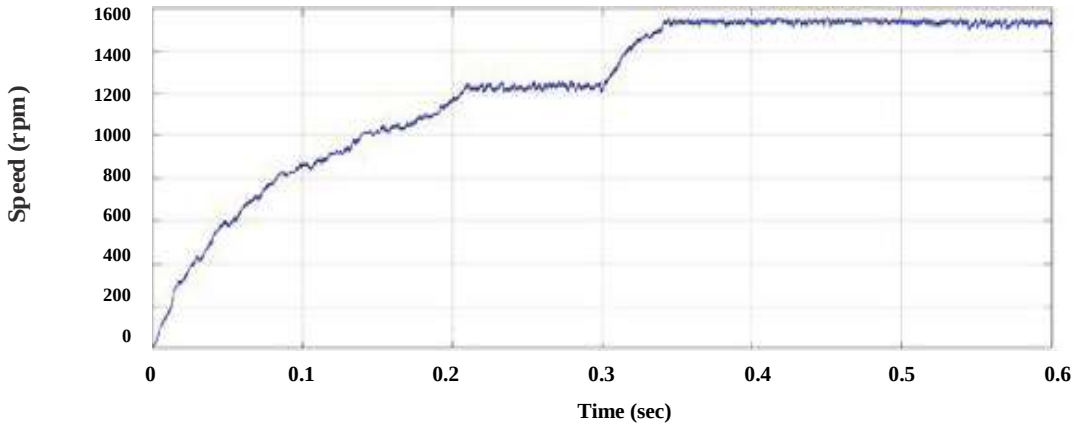


Fig.6.49 (b) : Output speed response using FOC-CB using 5KHz

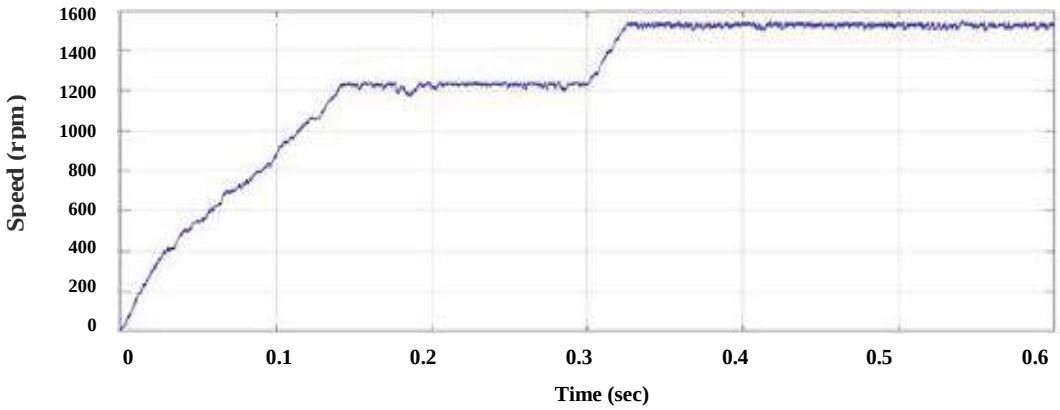


Fig. 6.49(c) : Output speed response using FOC-CB using 7.5KHz

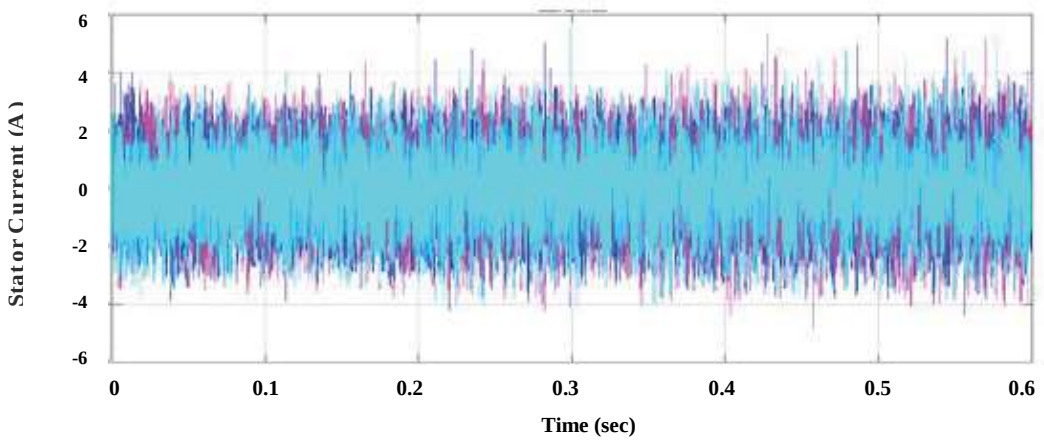


Fig. 6.50(a) : Output stator current response using FOC-CB using 2.5KHz

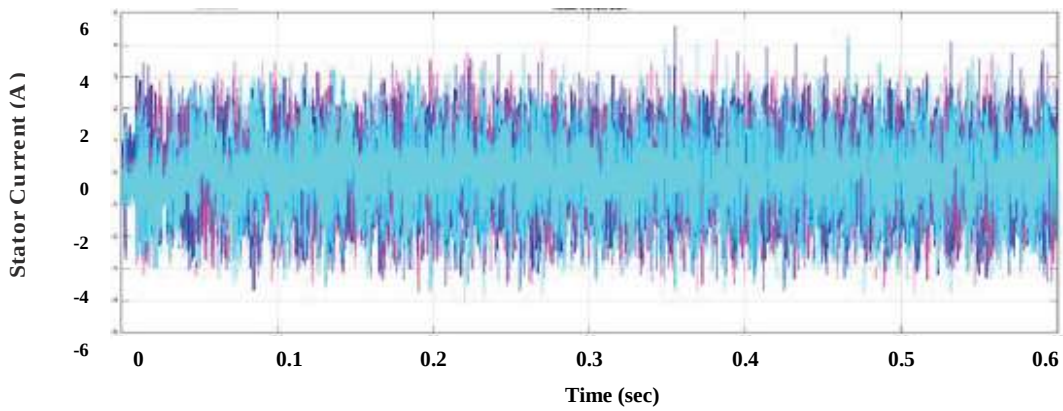


Fig. 6.50(b) : Output stator current response using FOC-CB using 5 KHz

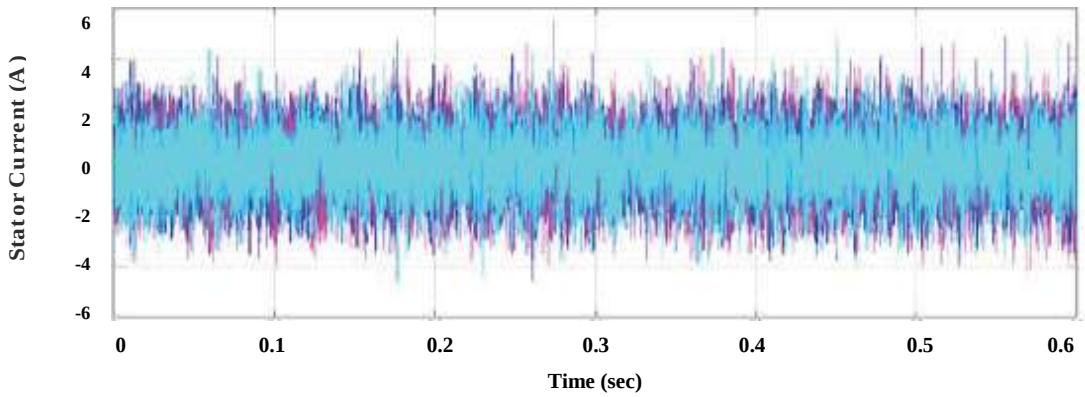


Fig. 6.50(c) : Output stator current response using FOC-CB using 7.5KHz

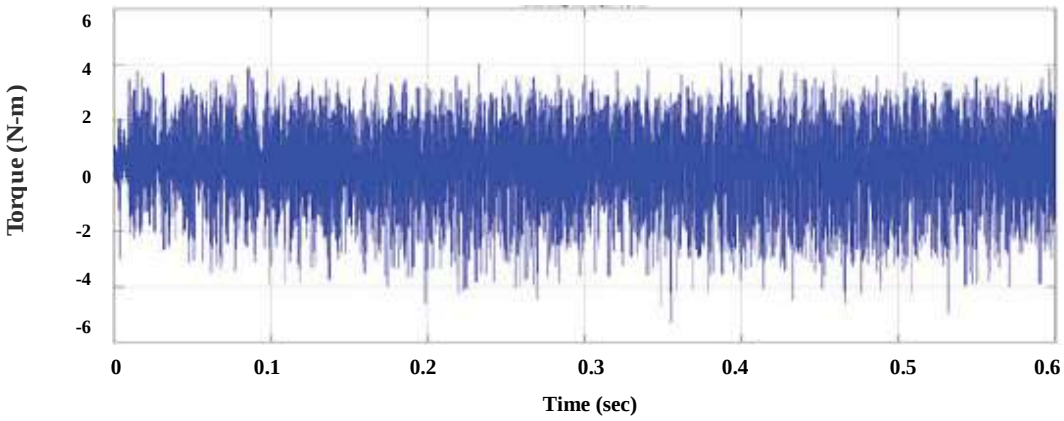


Fig.6.51 (a) : Output torque response using FOC-CB using 2.5KHz

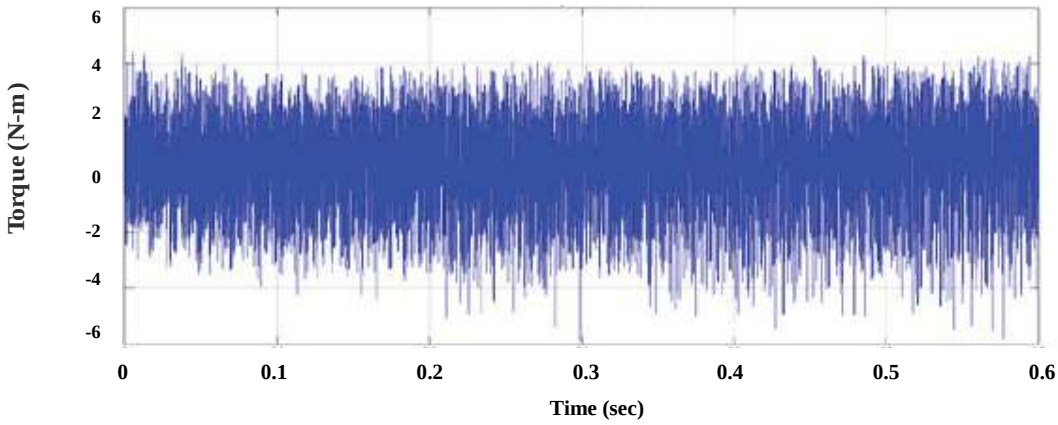


Fig.6.51 (b) : Output torque response using FOC-CB using 5 KHz

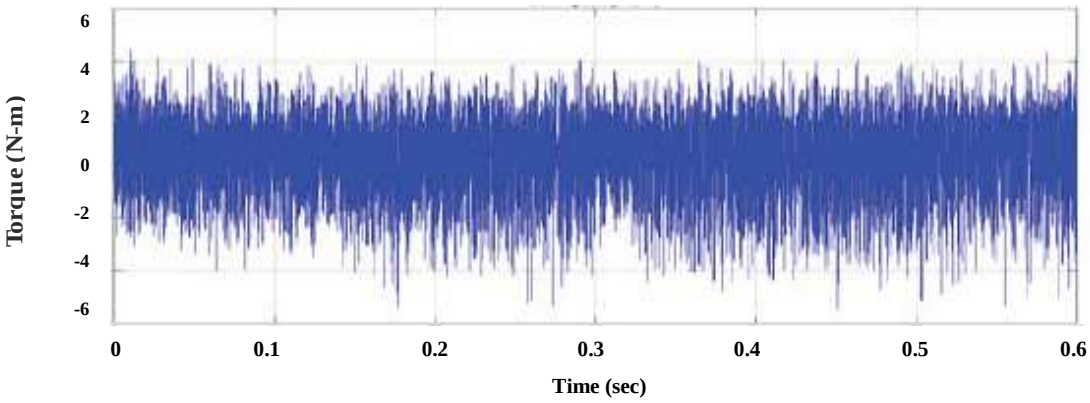


Fig. 6.51(c) : Output torque response using FOC-CB using 7.5KHz

Fig.6.49 (a),(b) ,(c) shows Output speed response using CB-FOC using 2.5KHz,5KHz and 7.5 KHz.Fig.6.50 (a),(b) ,(c) shows stator current response using CB-FOC using 2.5KHz,5KHz and 7.5 KHz.Fig.6.51 (a), (b), (c) shows Output torque response using CB-FOC using 2.5KHz,5KHz and 7.5 KHz.Fig.6.52 (a),(b) ,(c) shows Output speed response using CB-DTC using 2.5KHz,5KHz and 7.5 KHz. Fig.6.53 (a),(b) ,(c) shows Output stator current response using CB-DTC using 2.5KHz, 5KHz and 7.5 KHz. Fig.6.54 (a), (b), (c) shows Output torque response using CB-DTC using 2.5KHz,5KHz and 7.5 KHz.

6.12 ANALYSIS OF DTC-CB FED PMSM DRIVE AT DIFFERENT INVERTER SWITCHING FREQUENCIES

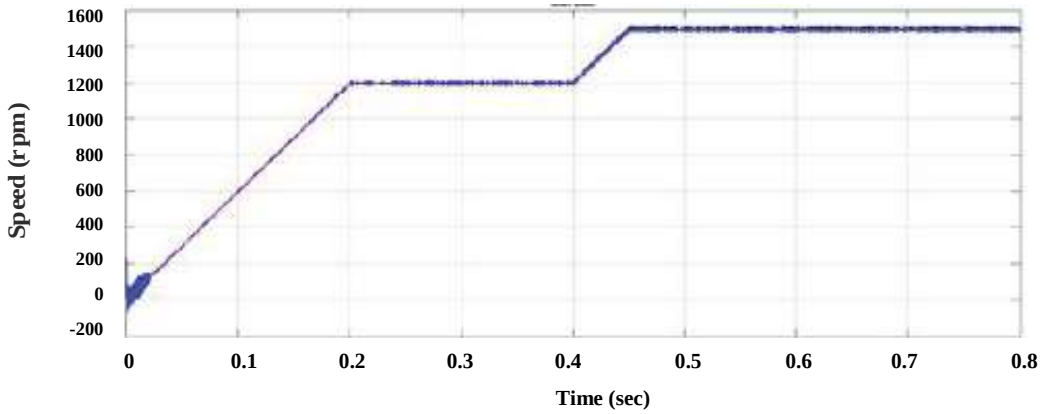


Fig.6.52 (a) : Output speed response using DTC-CB at 2.5KHz

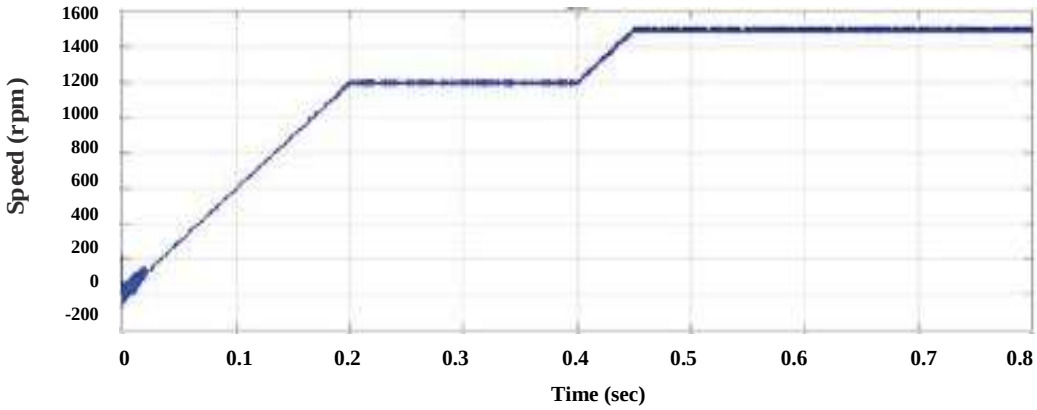


Fig.6.52 (b) : Output speed response using DTC-CB at 5KHz

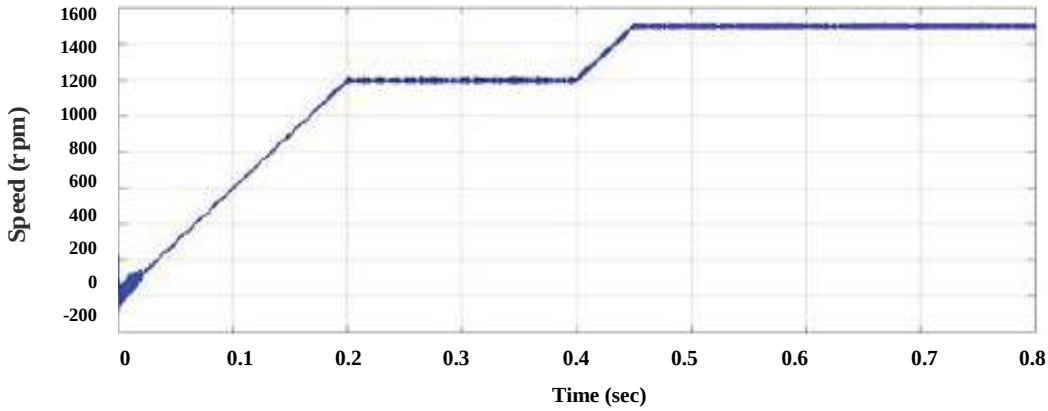


Fig.6.52 (c) : Output speed response using DTC-CB at 7.5KHz

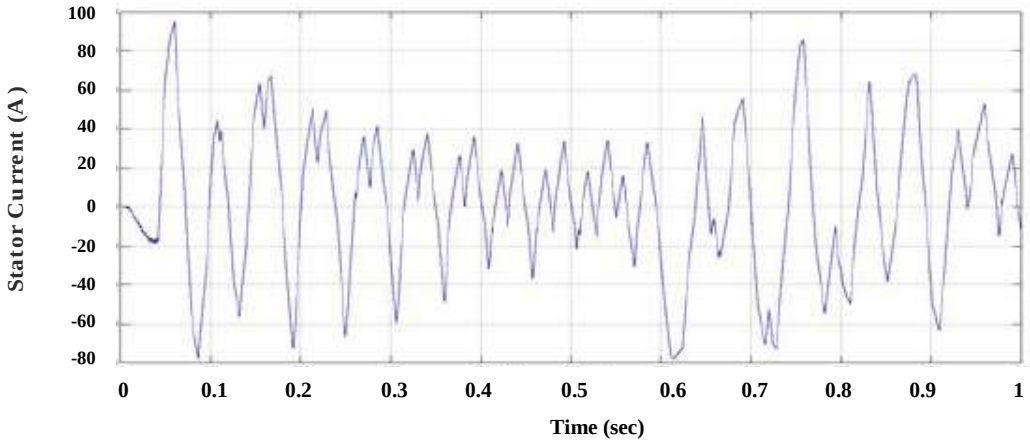


Fig. 6.53(a) : Output stator current response using DTC-CB at 2.5KHz

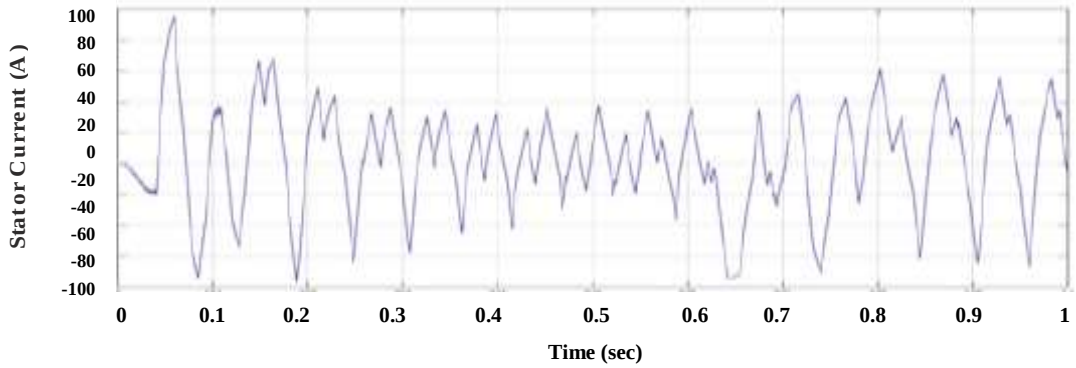


Fig. 6.53 (b) : Output stator current response using DTC-CB at 5 KHz

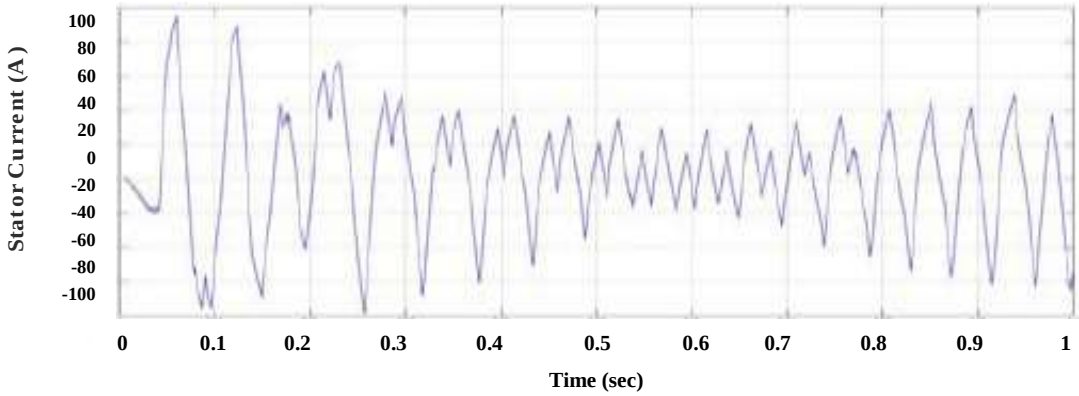


Fig. 6.53 (c) : Output stator current response using DTC-CB at 7.5KHz

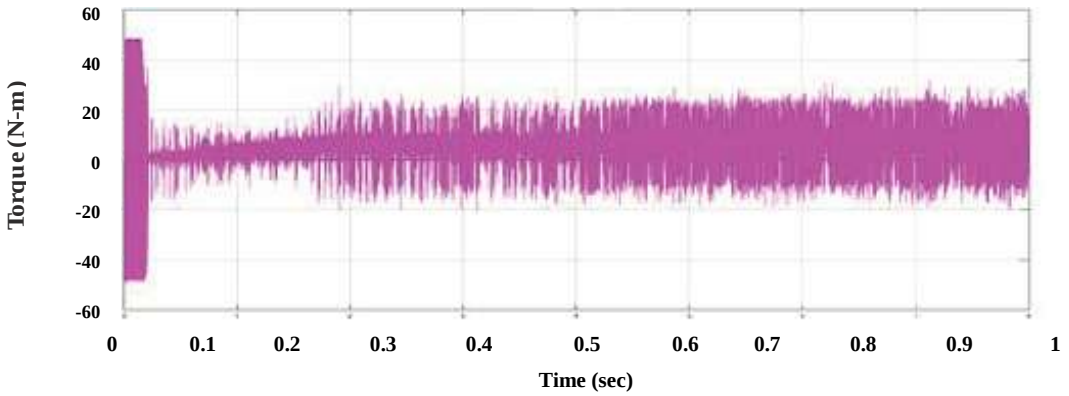


Fig.6.54 (a) : Output torque response using DTC-CB at 2.5KHz

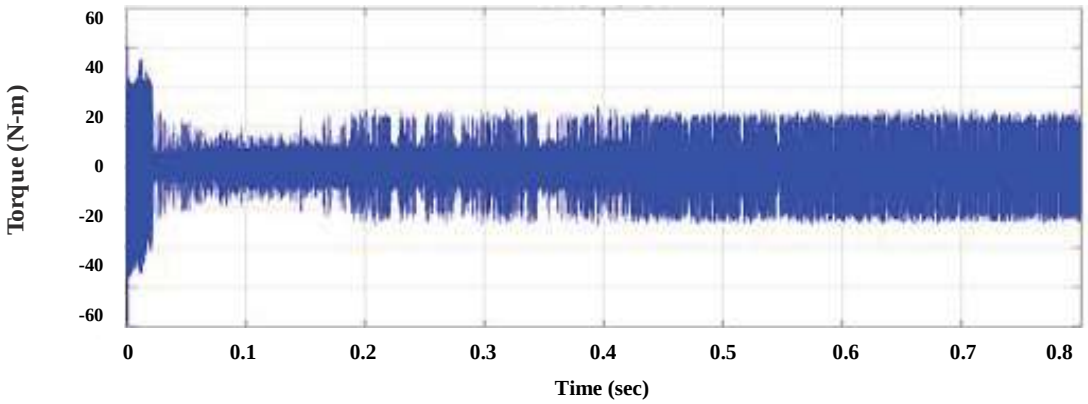


Fig.6.54 (b) : Output torque response using DTC-CB at 5 KHz

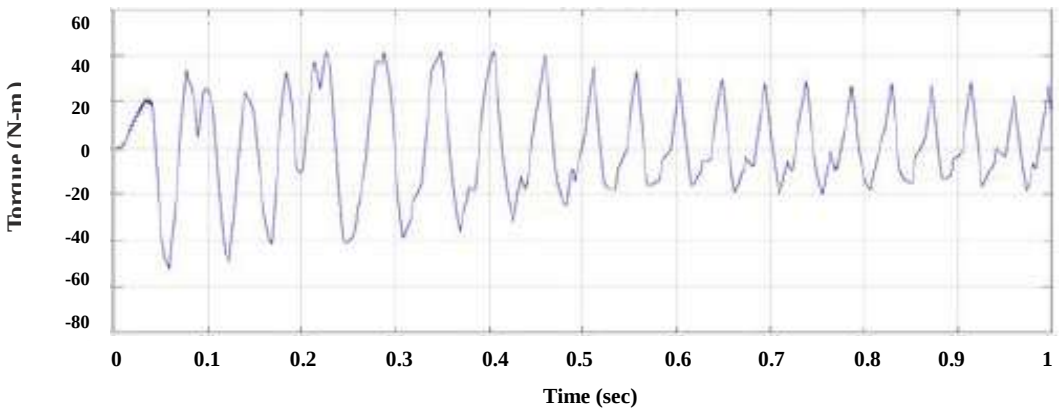


Fig. 6.54 (c) : Output torque response using DTC-CB at 7.5KHz

Fig.6.52 (a),(b) ,(c) shows Output speed response using CB-DTC using 2.5KHz,5KHz and 7.5 KHz.Fig.6.53 (a),(b) ,(c) shows Output torque response using CB-DTC using 2.5KHz,5KHz and 7.5 KHz. Table 6.6.Torque ripple and copper loss analysis of three level diode clamped inverter using FOC-CBSVM and DTC-CBSVM at different switching frequency

Copper losses can be computed as follows,

$$p_{cu} = (Ia^2 + Ib^2 + Ic^2) x R$$

Equal stator phase resistance was assumed (i.e. $Ra = Rb = Rc = R$).

Torque ripples Calculated by formula

$$\text{Torque ripple (\%)} = (Tmax - Tmin)/ Tavg * 100$$

Table 6.6 : Torque ripple analysis & copper loss of three level DCMLI at different switching frequencies

Speed(RPM)	Switching Frequency Range(KHz)	%Torque ripple		P_{cu}in watt	
		CB-FOC	CB-DTC	CB-FOC	CB-DTC
1200-1500 rpm	2.5 KHz	15.38%	**10.52%**	42.33W	**36.19W**
1200-1500 rpm	5 KHz	14.32%	**9.43%**	37.67W	**32.63W**
1200-1500 rpm	7.5 KHz	13.86%	**9.10%**	21.95W	**19.37W**

6.13 SIMULATION RESULT ANALYSIS

From fig 6.26 to fig 6.46 shows the steady state & transient performance of FOC and DTC based three level diode clamped inverter fed PMSM drive using CBSVM technique. From fig 6.49 to fig 6.51 shows the analysis of CB-FOC fed PMSM drive at different inverter switching frequencies. .From fig 6.52 to fig 6.55 shows the analysis of CB-DTC fed PMSM drive at different inverter switching frequencies. From all the outputs it is clear that DTC-CBSVPWM controller gives better performance compared FOC-CBSVPWM technique. it can also be extended to

n-level inverter as it is simple and easy to build. As the level increases the harmonics decreases, and better speed and torque response can be obtained.

Comparing the simulation results of the PMSM drive used in the Honda Civic 2006 hybrid electric vehicle under the control of the FOC and DTC control strategies using carrier based space vector modulation technique, we can get conclusions as the following.

- In FOC-CBSVM, due to the lower sampling period, the stator current is more sinusoidal using the hysteresis current control. But it needs the continuous rotor position information and the switching frequency of the three level diode clamped inverter is not constant. It causes torque and current ripples.
- In DTC-CBSVM, it does not need the rotor position information except for the initial rotor position. A novel carrier based space vector modulation technique using the switching table reduces current and torque ripples. Also maintained the switching frequency of the three level diode clamped inverter is constant.
- Comparing the simulation results of PMSM FOC and DTC drive under the control of switching table and carrier based space vector modulation techanique, we can conclude that the proposed carrier based space vector modulation technique with switching table can reduce the total harmonics of stator current and decrease current and torque ripples. In addition, switching frequency is fixed in DTC-CBSVM drive from this analysis we can conclude that direct torque control using CB-SVM for PMSM gives good dynamic performance as compare to FOC-CBSVM Hence DTC-CBSVM is validated for hardware implementation in automotive application.
- In the analysis of different switching frequency, It can be seen from the table 6.6, in each speed as the inverter switching frequency increased the copper losses and the torque ripples reduced.

- The results also showed that, the choice of the inverter in terms of lower torque ripples and lower copper losses do not only depend on the switching frequency but also on the motor speed.

Chapter 7 deals with detail design and implementation of DTC-CBSVM PMSM drive. Practical results obtained on the lab setup are presented.

CHAPTER – 7
HARDWARE IMPLEMENTATION OF DTC-CBSVM PMSM DRIVE

This chapter focuses on experimental system is designed to implement DTC-CBSVM of PMSM, design of PMSM drive and practical measurements results.

7.1 GENERAL HARDWARE OVERVIEW

Figure 1.5(chapter-1) shows a simple schematic diagram of the system. The equipments used in the lab setup of this research work are listed below:

- Permanent magnet synchronous machine.
- Three level diode clamped multilevel inverter (DCMLI).
- Voltage, current, rotor angle and speed measurement equipments.
- An AVR Microcontroller control system.
- 12V, 5V relay.
- An optocard(4N35) for Isolation.
- Various electrical items such as wires, connectors, grounding and so on.

All these equipment are installed in the following way:

- A measurement box that includes:
  - A hall sensor (ACS712-5A) for current measurements.
  - A hall sensor (A3144) that measures rotor angle and speed.
  - Connector terminals to electrically link different components.
- The inverter box which includes:
  - A voltage source that supplies the inverter control system.
  - A three leg switch-mode inverter that uses IGBT switches.
  - A designed electronic board to drive the relay
- Three phase delta connected Permanent magnet Synchronous Motor.

- Control system is based on the AVR Microcontroller, including the following parts:
  - ATMEGA8 board for generation of gate pulses
  - ATMEGA16 board for sensing, monitoring & control various parameters such as current, voltage, rotor speed and angle, etc

7.2 DESIGN OF PMSM DRIVE

7.2.1 Design of diode bridge rectifier and filter circuit

Input line voltage	=	280 Vac
Output dc voltage	=	380 vdc
Load current	=	2.2 Amp.
Vm	=	$\sqrt{2}$ x 280
	=	396v
Vdc	=	2 Vm/π = 2 x 396 /π
	=	252 (without filter)

But with Capacitor filter

V_{dc} required	=	396 v
V_{dc}	=	V_m – (Vrpp/2)
380	=	396 – (Vrpp/2)
∴ V_{rpp}	=	32 v
$V_{r\ rms}$	=	Vrpp/2 √3
	=	9.35v
∴ r	=	V_{rms}/vdc
	=	9.35/380
	=	0.024
c	=	¼ √3f. r. Rs
	=	¼ √3 x 50 x 0.024 x 300
	=	406 μf
Selected two capacitor		C_1 = 470 μf, 400 v
		C_2 = 470 μf, 400 v

And are connected in series to get total 406 μf we have

$V_{ac\ (max)} = V_m = 396$ v

$V_{o\ (min)} = V_m = V_m - V_{rpp}$

$= 396 - 32$

$= 364$v

$\theta = \sin^{-1} V_0(min) / V_0\ (max)$

$= \sin^{-1} \times 364 / 396$

$= 66.80^0$

diode conduction angle $= 90 - \theta$

$= 90 - 66.80^0$

$= 23.19^0$

I_p (surge current) $= T/T_1 \times Idc$

$= 360^0 / 23.19^0 \times 2.2$

$= 34.15$ A

Diodes:-

V_R (max) $> V_m$

> 396 Volts

I_f (ave) $> I_0$

> 2.2 A

Isurge $> I_p$

> 34.15 A

selected diode are D_1 to D_8 = 1N5408

Two diodes Connected in parallel for double current flow.

Specification:

1.	Maximum Average Forward Rectified Current (Iav)	3 A
2.	Maximum Recurrent Peak Reverse Voltage (Vrrm)	400 V
3.	Maximum DC Blocking Voltage (Vdc)	400 V

7.2.2 Design of main power circuit

IGBT bridge

While selecting IGBT

V_{dc} > 0.707 x m_a Vdc [let m_a = 1 (max)]

> 0.707 x 1 x 380

> 268.66 volts

V_{gs} > 12 volts

I_d > I_L max

> 2 Amps

Switching time should be as small as possible selected IGBT is FGA15N120A

Specifications

1.	Drain-Source Voltage	1200 V
2.	Gate-Source Voltage	+20V/-20V
3.	Continuous Drain Current	15 A
4.	Turn-Off Delay Time	160 ns
5.	Fall Time	100 ns

Snubber Circuit

From data sheet of IGBT

Turn off delay = 160 ns, Fall time = 100 ns

Let to be design for maximum current capacity of IGBT i.e. 15 Amps

C = I_0 T off / 2 V_d

= 20 x 260 ns / 2 x 268.66

= 0.009 μF

For better performance large capacitor C to be selected. So that IGBT voltage rises slowly and takes longer time to reach peak value of voltage capacitor C_7 to C_{14} are selected as 0.01μF, 1KV each. The maximum load current is taken to be 15 A and maximum voltage reading of IGBT is 1200 volt,

I_f (ave) = 15 A

V_K = 1200 V

Inverter Output Voltage = 270 V (Line-Line)

Input DC rectified current (max.) = 6 A

Power Rating of Inverter = 1500 VA

= 1.5 KVA

Switching Frequency = 2.5 KHz (400 us)

No. of Clamed Diode require = (m-1) (m-2)

where, m is no. of level of inverter (m = 3)

= 2 (per phase)

Clamped Diode Used (D9 to D14) is IN5408.

Specification of Clamed diode:

1.	Maximum Average Forward Rectified Current (Iav)	3 A
2.	Maximum Recurrent Peak Reverse Voltage (Vrrm)	400 V
3.	Maximum DC Blocking Voltage (Vdc)	400 V

7.2.3 Design of Isolator and driver circuit

i) Design of Opto coupler

Selected opto Coupler is 4N35 which has got IRED and phototransistor internally. The maximum forward current for LED = 20 mA

Peak output voltage of ATMEGA8 will be = 5 v

Let maximum current for LED to be selected as 20 mA

R = V_i / I_f

= 5 / 20 mA

= 250 Ω

Selected R = 270 Ω ¼ w

With this value

I_f (max) = 5 / 270Ω

= 18.5 mA

which is acceptable value for 4N35.

selected R_{20} to R_{23} & R_{44} to R_{47} = 270 Ω ¼ w each.

4N35 requires supply voltage = 12 Vdc

So we design power supply for the rating 100 mA.

Using transformer of 12-0 secondary voltage.

V_m (sec) = √2 x 12 = 17 V

Selected ripple voltage V_{rpp} = 0.5 V

For same voltage, at any input range of AC supplie we used a regulator IC as 7812

Hence Vdc = 12 V

Spécification of 4N35

1.	Collector emitter breakdown voltage	70 V
2.	Collector current	100 mA
3.	Forward current	20 mA
4.	Reverse voltage	6 V

Diodes:

PIV > Vm

> 17 V

I_f > I_1

> 500 mA

Selected diodes D_{15} to D_{39} are IN4007

1.	Maximum Average Forward Rectified Current (Iav)	1 A
2.	Maximum Recurrent Peak Reverse Voltage (Vrrm)	1000V
3.	Maximum DC Blocking Voltage (Vdc)	1000 V

ii) Transformer

Transformer used here is a signal core six isolated secondary with rating 12-0-12, 500 mA each.

7.3 SYSTEM VALIDATION

7.3.1 Introduction

Fig.1.5. (Chapter-1) shows the block diagram of the laboratory model. The main part of the systems is a PMSM, the specification of which has been given in table.7.1. The magnetic flux created by the permanent magnets has a fixed value. For PMSM, the inductances in direct and quadrature axes are the same values. The diode clamped inverter requires twelve gate pulses for triggering the IGBT's. A triggering

circuit comprises of AVR Microcontroller, optocouplers(4N35) and FGA15N120AN IGBT's drivers has been designed and constructed. AVR Microcontroller has been programmed to generate the twelve pulses for the IGBT's power circuit. Two ports i.e. port B and port C, have been used to channel the signals to the IGBT's. As a protection for the microcontroller between the high voltage and low voltage devices, 4N35 optocouplers have been selected as the isolation devices. Single channel IGBT's driver FGA15N120AN has been chosen as the driver to provide the required voltage and power to switch on and off the IGBT's. It also functions as an isolation device. The AVR Micro controller is used to generate pulse using CB-SVPWM technique for three-level DCMLI. Fig.7.1 .shows the power circuit of the 3-level diode clamped multilevel inverter. The converter is designed for following specification:

Input Voltage (Three phase)	V_{in} = 280 V (rms)
Supply Frequency	f_{in} = 50 Hz
Output Voltage with filter (Rectifier)	V_r = 380 V dc
Output rms Voltage (Inverter)	V_o = 270 V (Line-Line)
Switching Frequency	f_s = 2.5 KHz
Inverter Rating (KVA)	P_o = 1.5 KVA
Resistive load	180 Watts

Table 7.1 : PMSM parameters

Power	P	0.5 H.P(373W)
Number of pole pairs	P	2
Phase current	I(rms)	1.5 A
Phase voltage	U(rms)	160V
Magnetic flux-linkage	ΨPM	0.1852Wb
Rotor speed	Ωm	1500 rpm
Nominal torque	Me	4 N-m
Moment of the inertia	J	0.0001854 kgm^2
Stator winding resistance	Rs	1.6 Ω
Stator d-axis inductance	Ld	0.006365
Stator q-axis inductance	Lq	0.006365

7.3.2 Power Circuit of Three Level Diode Clamped Inverter

This circuit converts the available ac line voltage into required dc voltage for the twelve switch diode clamped inverter. It uses eight diodes D_1, to D_8 in bridge configuration as shown in fig.7.1.Diode bridge converts ac to dc. This dc voltage is not pure dc voltage but contains ac ripples in it. So capacitor is connected across the output of the bridge rectifier which filters out ac contained in the dc and gives almost pure dc voltage. Fig.7.1 shows the Power circuit of twelve switch diode clamped inverter fed PMSM drive, where only one DC source Vd is needed. Two capacitors are used to split the DC voltage and provide a neutral point N. The inverter leg A is composed of four active switches Sa1, Sa2, Sa3 and Sa4 with two anti-parallel diodes D9 to D10. The switches are employed with 12 IGBT's .Switching states for three-level inverter are shown in Table.7.2. Table 7.3. shows the output phase and Line-to-Line voltages of 3-Level Diode Clamped InverterFor one leg operation of phase-A for a three-level diode clamped inverter, to have a output voltage of Vdc/2 the switches Sa1, Sa2 should conduct and to have –Vdc/2 voltage, the switches Sa3. Sa4 should conduct and to have output voltage as zero the switches Sa2, Sa3 should conduct. For each voltage level two switches should conduct at a time. The maximum output voltage in the output is half of the DC source.

Table 7.2 : Switching sequences for three-level diode clamped inverter

Sector	Voltage Vector	Switching State											
		Sa1	Sa2	Sa3	Sa4	Sb1	Sb2	Sb3	Sb4	Sc1	Sc2	Sc3	Sc4
1	V1	1	1	0	0	0	0	1	1	0	0	1	1
2	V2	1	1	0	0	0	1	1	0	0	0	1	1
3	V3	1	1	0	0	1	1	0	0	0	0	1	1
4	V4	0	1	1	0	1	1	0	0	0	0	1	1
5	V5	0	0	1	1	1	1	0	0	0	0	1	1
6	V6	0	0	1	1	1	1	0	0	0	1	1	0
7	V7	0	0	1	1	1	1	0	0	1	1	0	0
8	V8	0	0	1	1	0	1	1	0	1	1	0	0
9	V9	0	0	1	1	0	0	1	1	1	1	0	0
10	V10	0	1	1	0	0	0	1	1	1	1	0	0
11	V11	1	1	0	0	0	0	1	1	1	1	0	0
12	V12	1	1	0	0	0	0	1	1	0	1	1	0

Table 7.3 : Output Phase voltages and Line-to-Line Voltages of 3-Level Diode Clamped Inverter

Sector	Phase Voltage			Line Voltages		
	Vab	Vbc	Vca	Van	Vbn	Vcn
1	(2/3)Vs	-Vs/3	-Vs/3	Vs	0	-Vs
2	Vs/2	0	-Vs/2	Vs/2	Vs/2	-Vs
3	Vs/3	Vs/3	-(2/3)Vs	0	Vs	-Vs
4	0	Vs/2	-Vs/2	-Vs/2	Vs	-Vs/2
5	-Vs/3	(2/3)Vs	-Vs/3	-Vs	Vs	0
6	-Vs/2	Vs/2	0	-Vs	Vs/2	Vs/2
7	-(2/3)Vs	Vs/3	Vs/3	-Vs	0	Vs
8	-Vs/2	0	Vs/2	-Vs/2	-Vs/2	Vs
9	-Vs/3	-Vs/3	(2/3)Vs	0	-Vs	Vs
10	0	-Vs/2	Vs/2	Vs/2	-Vs	Vs/2
11	Vs/3	-(2/3)Vs	Vs/3	Vs	-Vs	0
12	Vs/2	-Vs2	0	Vs	-Vs/2	-Vs/2

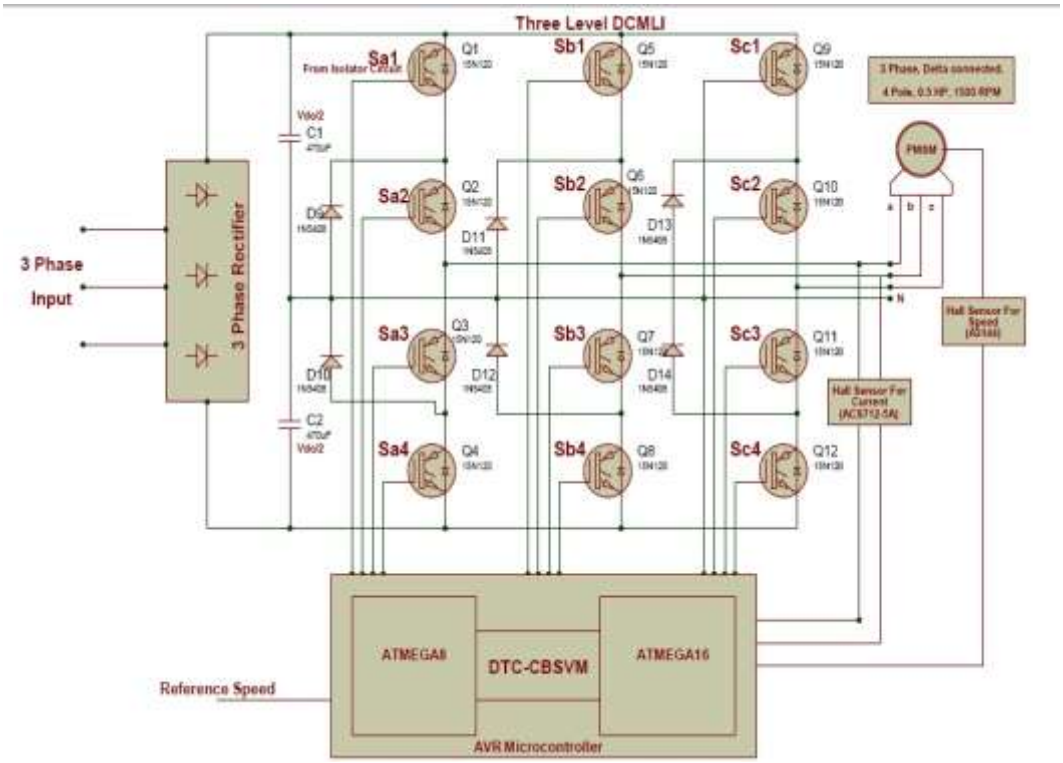


Fig.7.1 : Power circuit of Twelve Switch Diode Clamped Inverter fed PMSM drive

7.3.3 Description of Control Circuit of AVR Microcontroller

- **ATmega16** is an 8-bit high performance microcontroller of Atmel's Mega AVR family with low power consumption. Atmega16 is based on enhanced RISC (Reduced Instruction Set Computing, Know more about RISC and CISC Architecture) architecture with 131 powerful instructions. Most of the instructions execute in one machine cycle. Atmega16 can work on a maximum frequency of 16MHz.

  ATmega16 has 16 KB programmable flash memory, static RAM of 1 KB and EEPROM of 512 Bytes. The endurance cycle of flash memory and EEPROM is 10,000 and 100,000, respectively. ATmega16 is a 40 pin microcontroller. There are 32 I/O (input/output) lines which are divided into four 8-bit ports designated as PORTA, PORTB, PORTC and PORTD. ATmega16 has various in-built peripherals like USART, ADC, Analog Comparator, SPI, JTAG etc. Each I/O pin has an alternative task related to in-built peripherals. The following table shows the pin description of ATmega16.

- **ATmega8** is an 8-bit high performance microcontroller of Atmel's Mega AVR family with low power consumption. Atmega16 is based on enhanced RISC (Reduced Instruction Set Computing, Know more about RISC and CISC Architecture) architecture with 131 powerful instructions. Most of the instructions execute in one machine cycle. Atmega8 can work on a maximum frequency of 16MHz. Atmega8 has 8 KB programmable flash memory, static RAM of 1 KB and EEPROM of 512 Bytes. The endurance cycle of flash memory and EEPROM is 10,000 and 100,000, respectively.

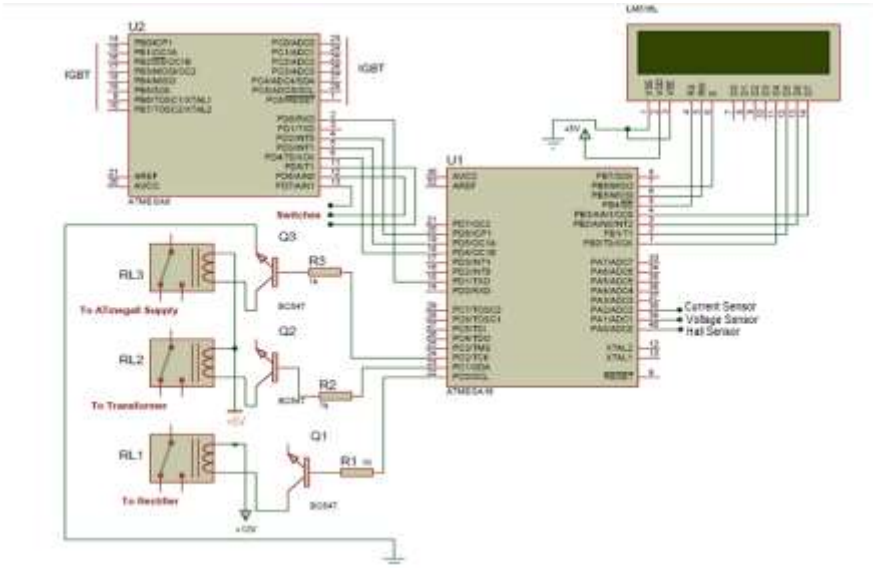


Fig 7.2 : Interfacing Diagram of Atmega16 & ATmega8

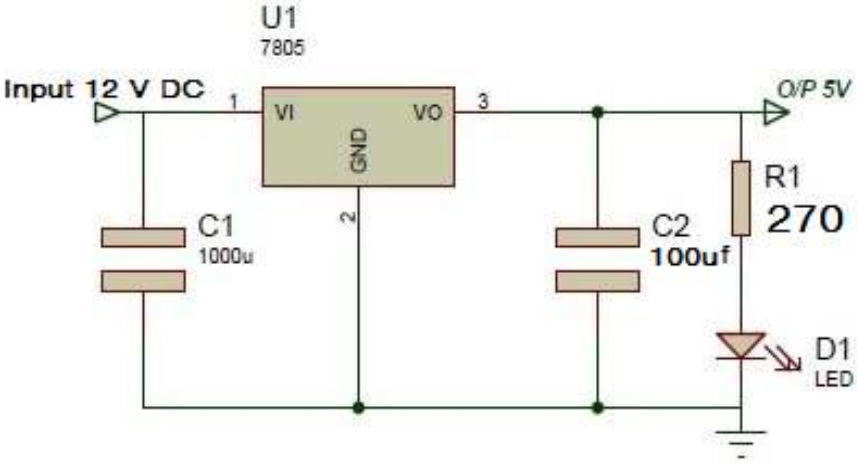


Fig 7.3 : Power Circuit for ATMEGA16 Board

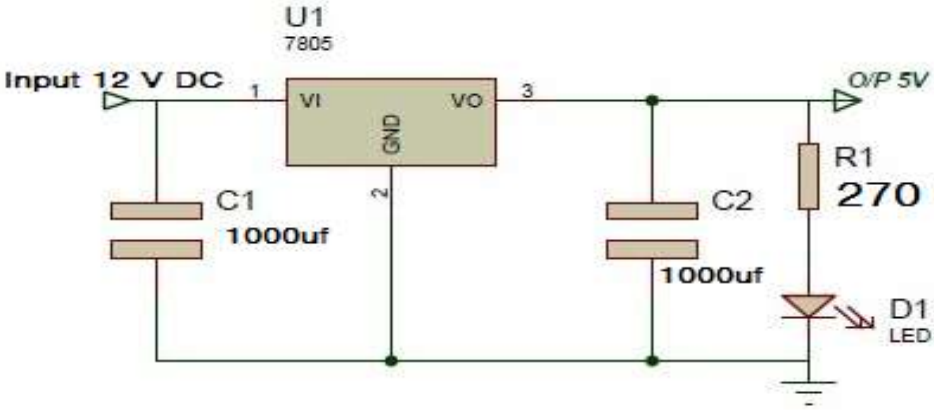


Fig 7.4 : Power Circuit for ATMEGA8

7.3.4 Flow chart of PMSM drive

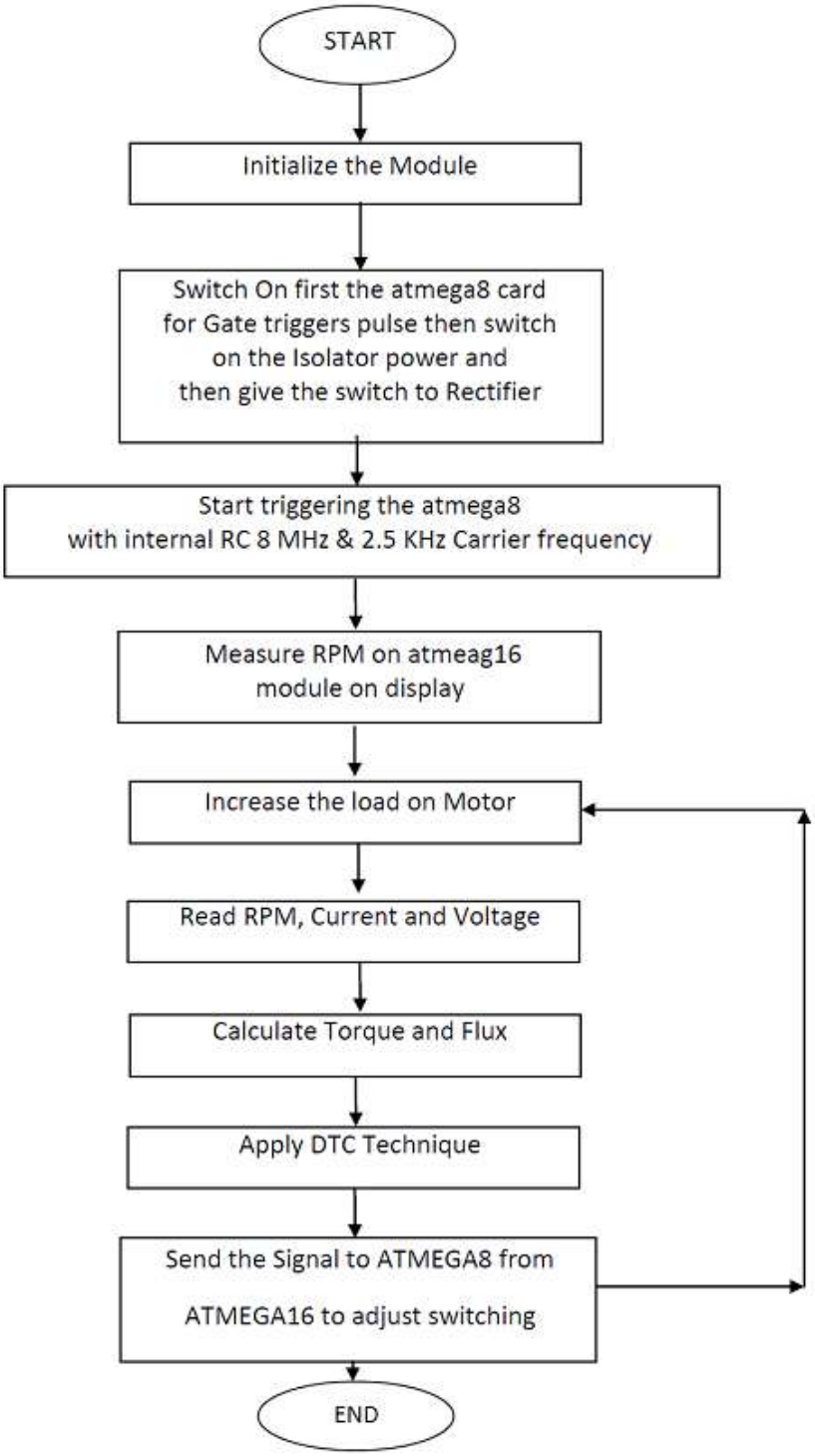


Fig 7.5 : Flow chart of PMSM drive

7.4 EXPERIMENTAL SETUP OF PMSM DRIVE

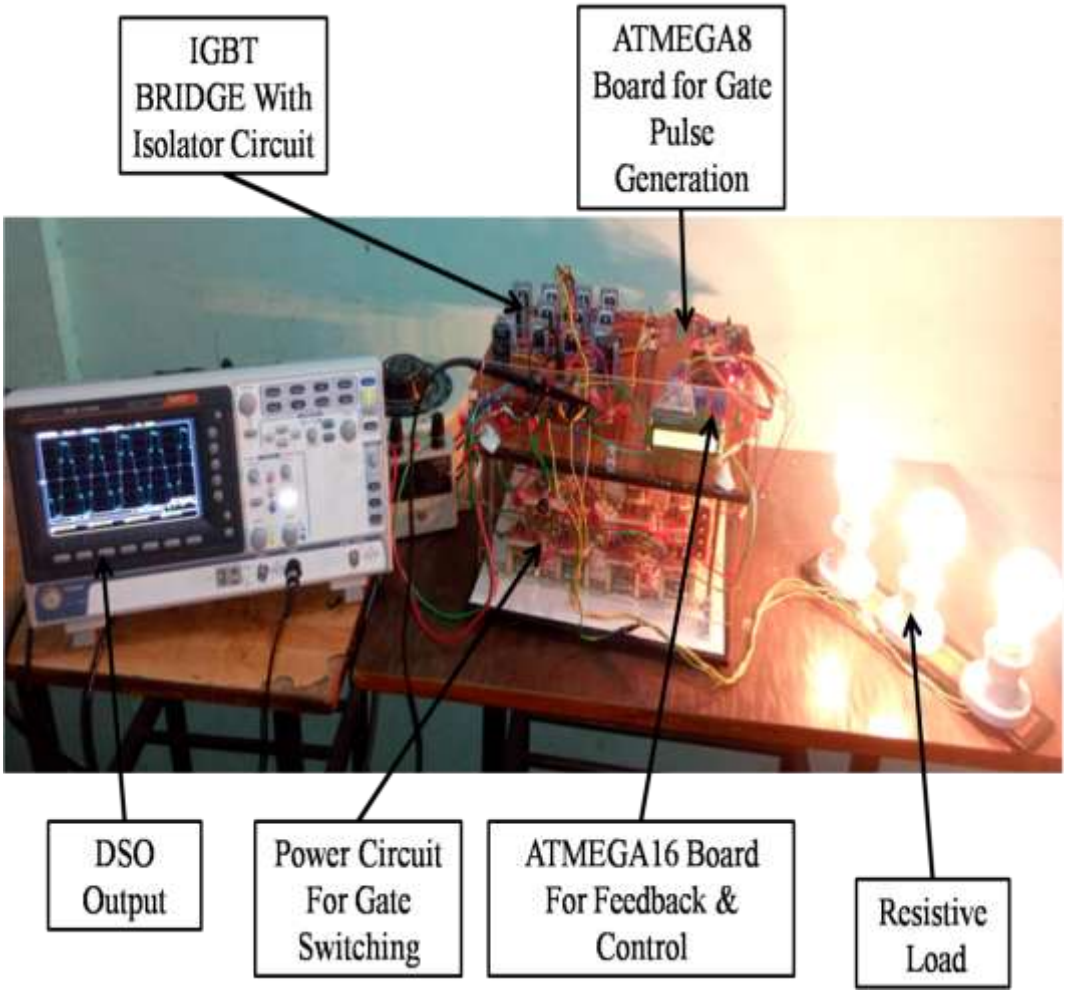


Fig. 7.6.a. : Experimental setup for PMSM drive with resistive loading

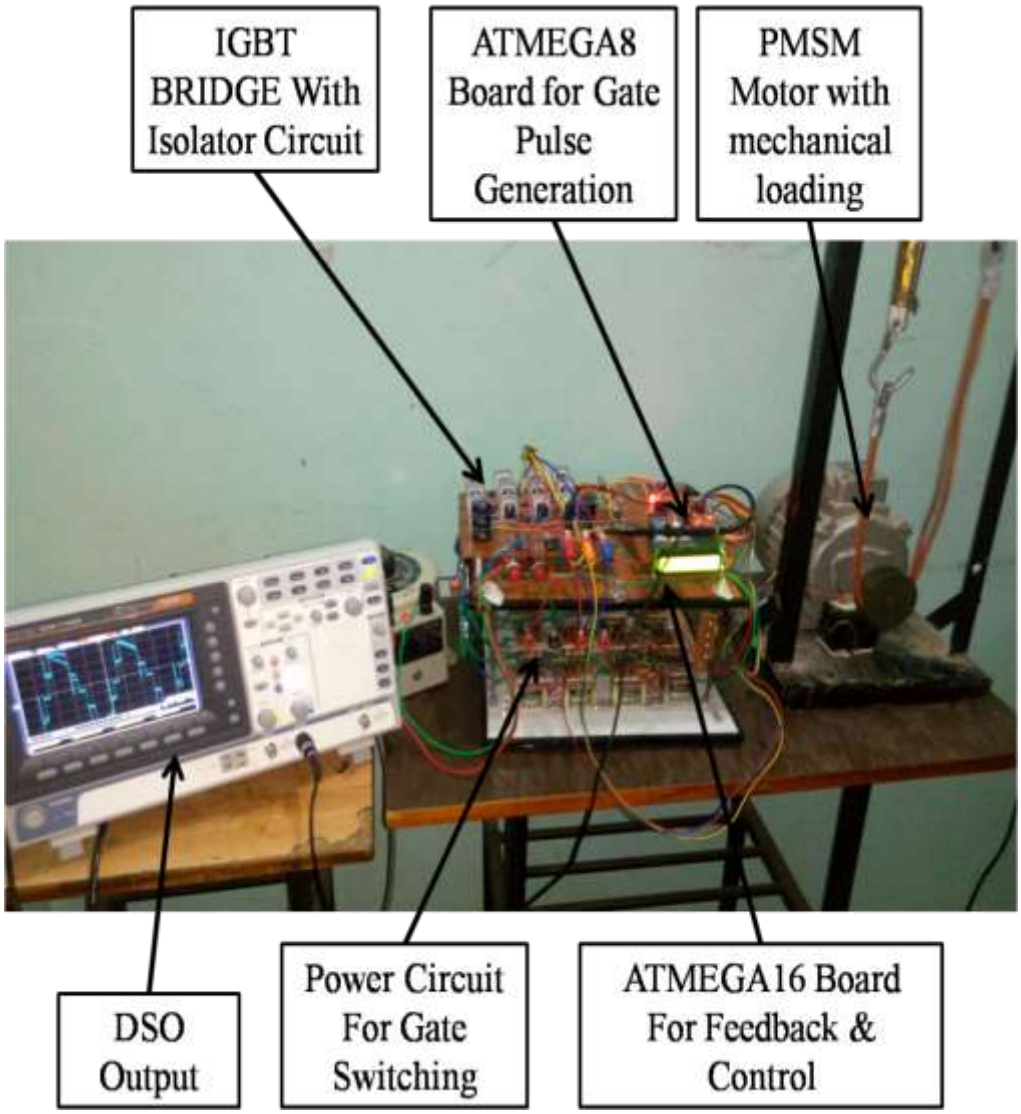
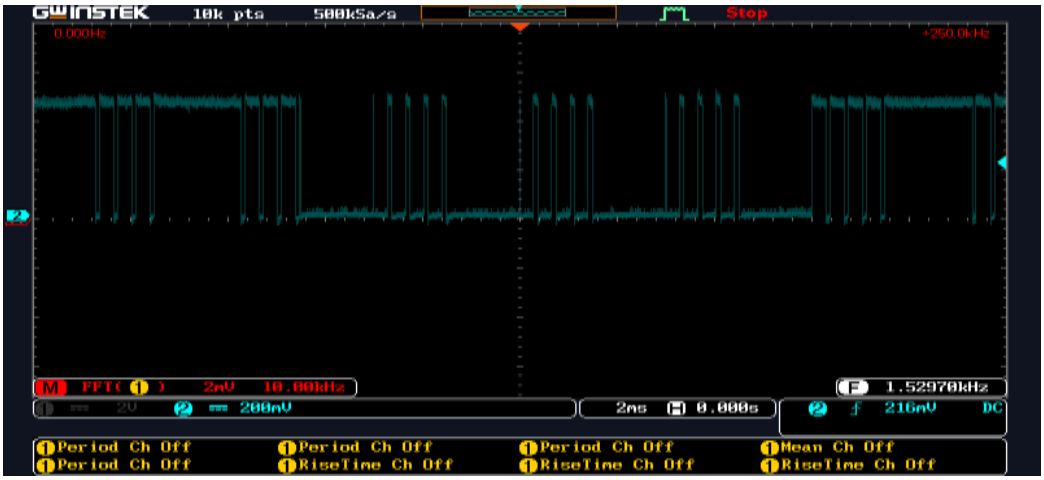


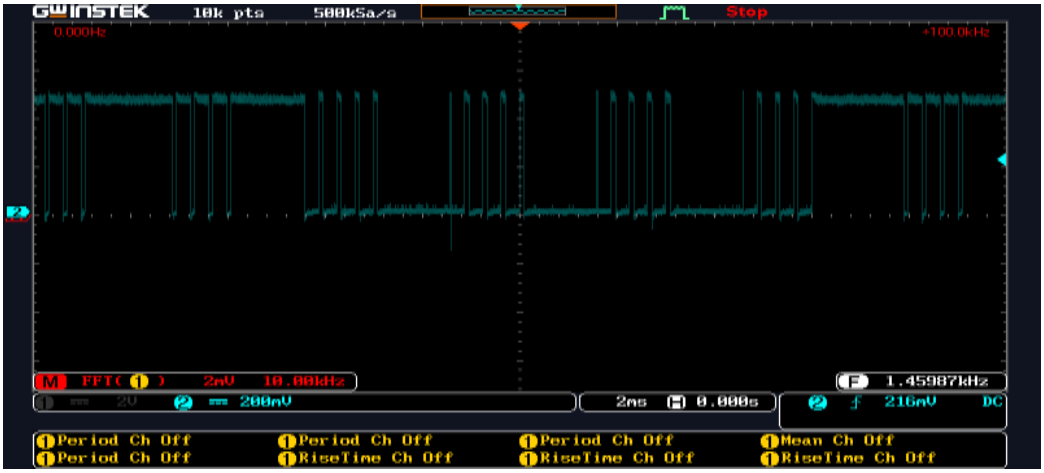
Fig. 7.6.b : Experimental setup for PMSM drive with mechanical loading

7.5 EXPERIMENTAL RESULTS AND ANALYSIS

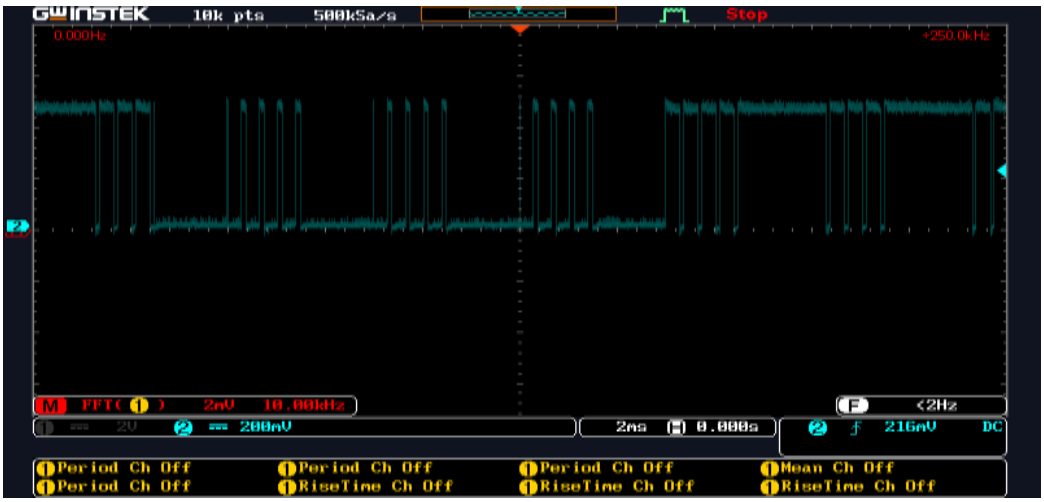
The photo of laboratory setup is presented in Fig.7.6(a) and Fig.7.6(b) , The algorithm in fig.7.5 is implemented using AVR microcontroller platform and the experimental results are presented for a three–level diode clamped multilevel inverter(DCML) as shown in Fig. 7.9 to Fig 7.14. The experiment is done under the following conditions: DC link = 380 V is used for the inverter, output voltage fundamental harmonic f = 50 Hz, switching frequency $f$sw = 2.5 kHz, and a three-phase 1.5 KVA, unity power factor load.



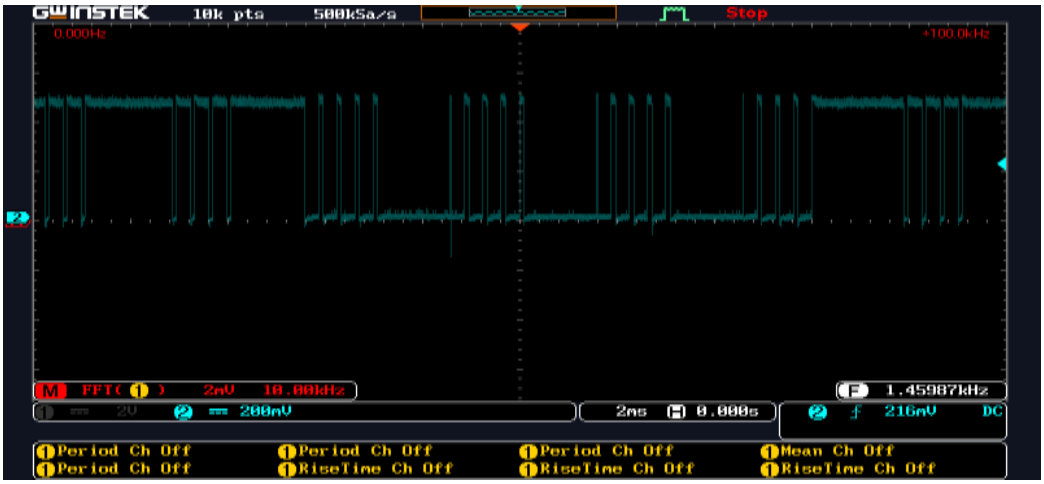
Gating pulse Sa1



Gating pulse Sa2

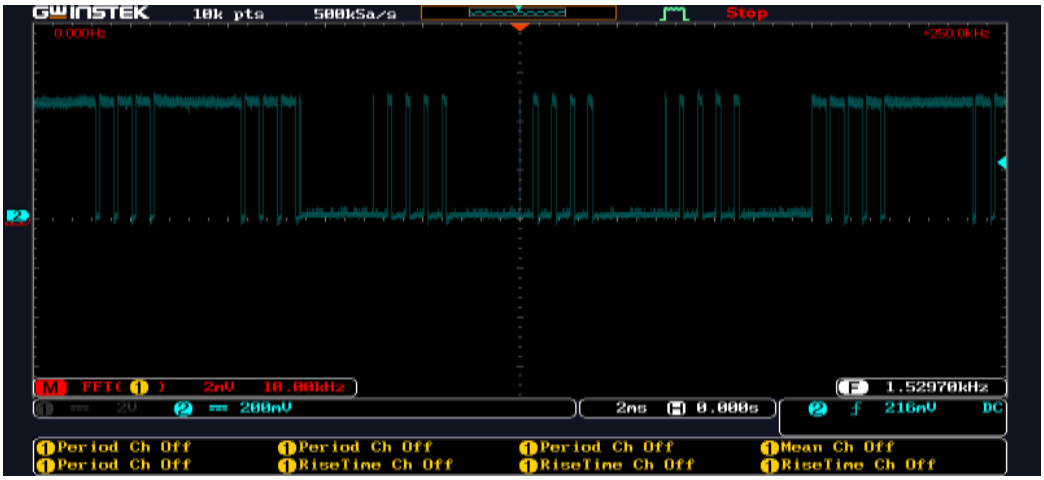


Gating pulse Sa3

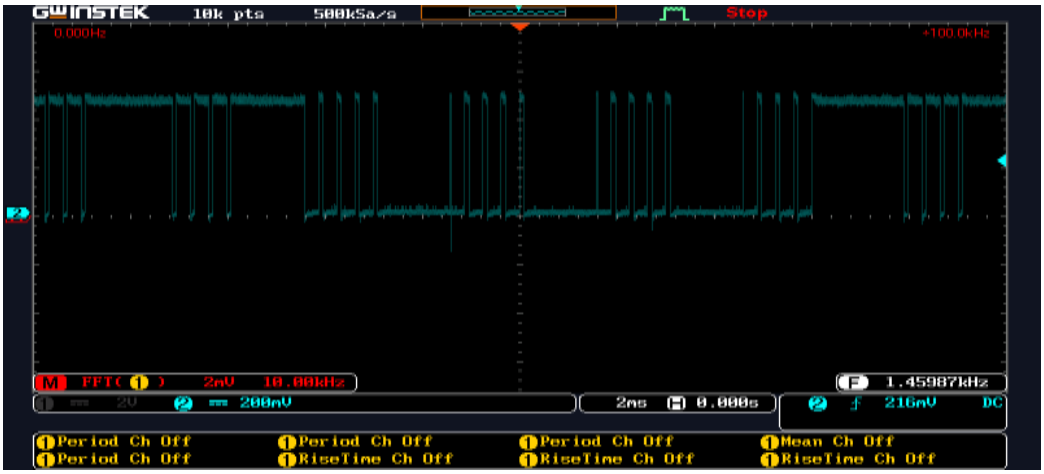


Gating pulse Sa4

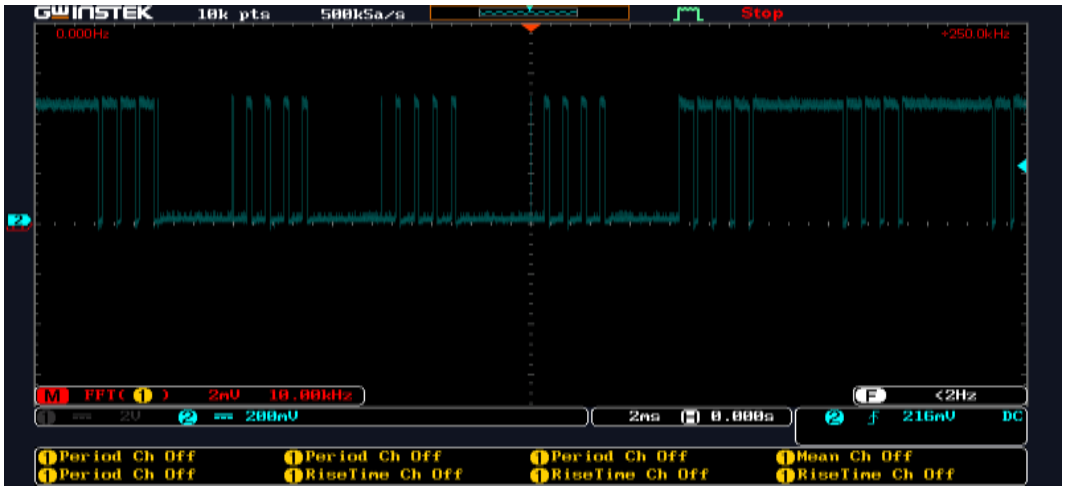
Fig.7.7.a Gating pulse of Lag A



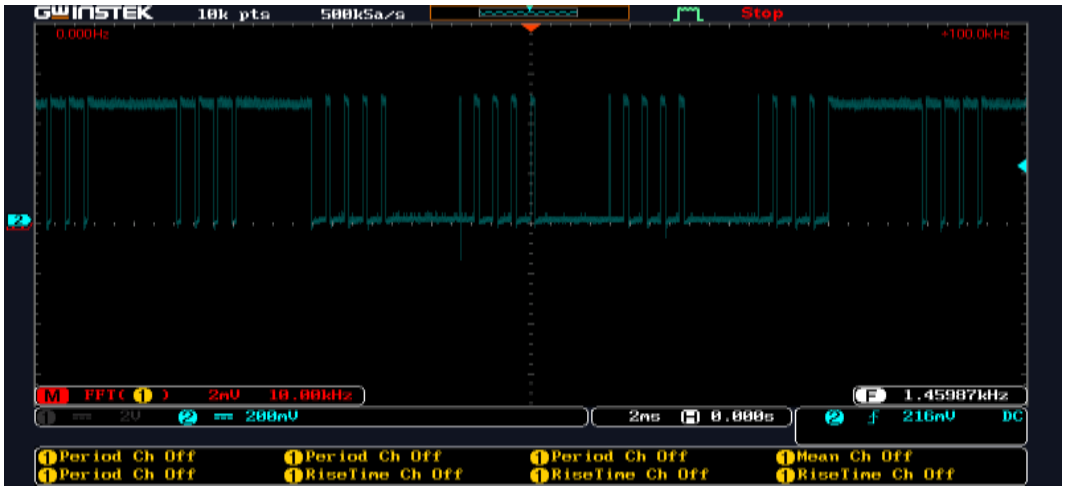
Gating pulse Sb1



Gating pulse Sb2

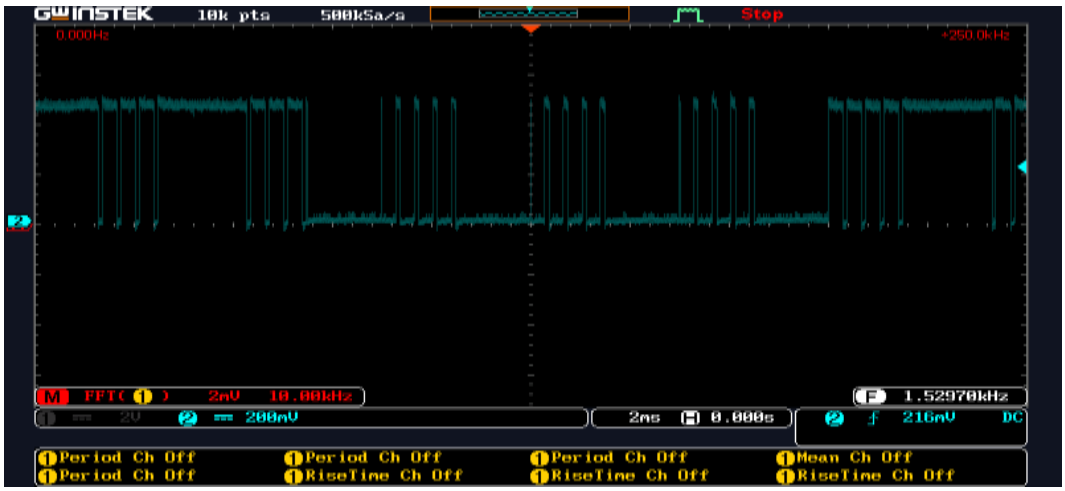


Gating pulse Sb3

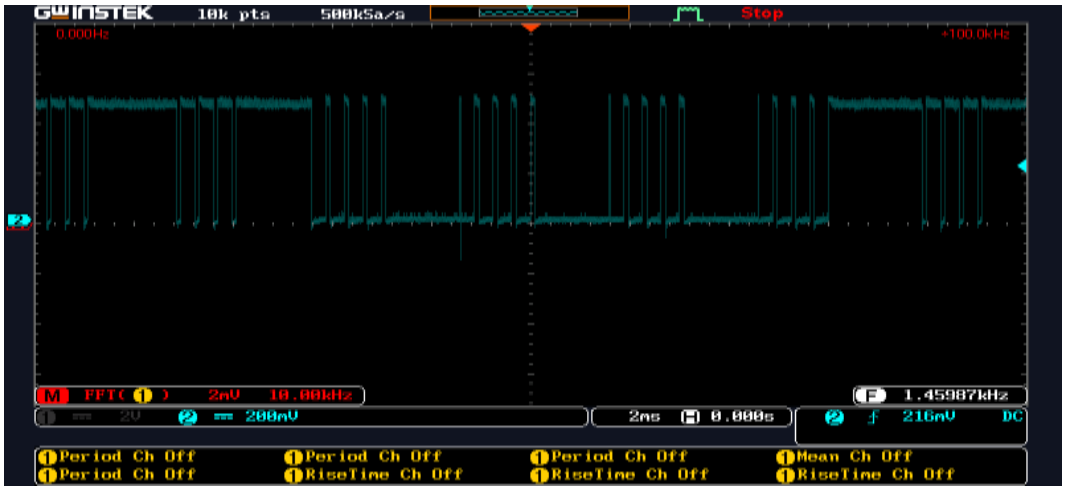


Gating pulse Sb4

Fig.7.7.b Gating pulse of Lag B

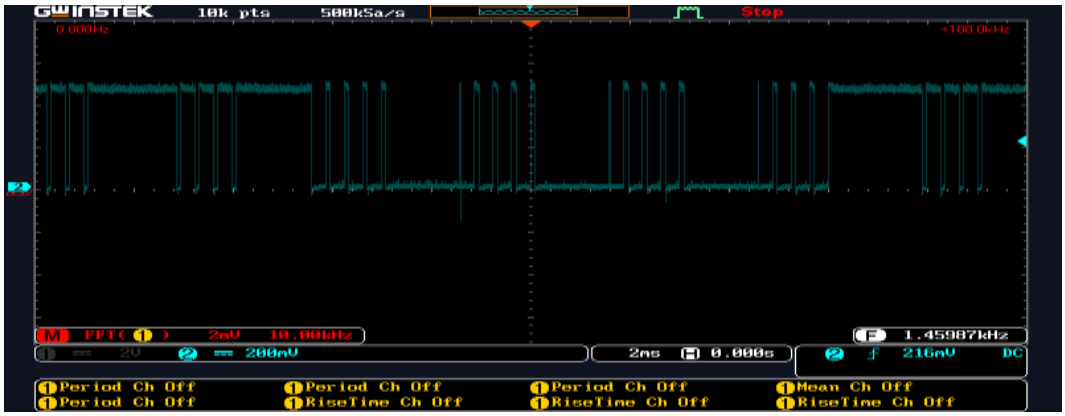


Gating pulse Sc1



Gating pulse Sc2

Gating pulse Sc3



Gating pulse Sc4

Fig.7.7.c : Gating pulse of Lag C

Fig. 7.7 : Typical operating waveforms of the practical three phase diode clamped inverter with gating pulse

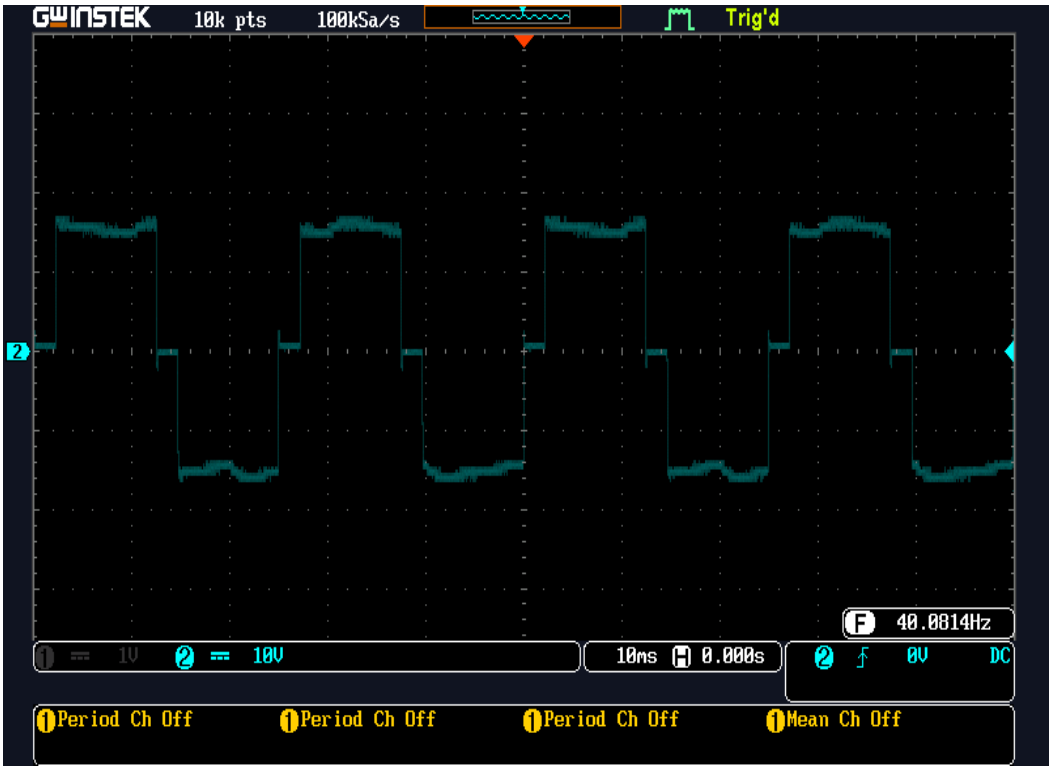


Fig. 7.8 Experimental waveforms for phase to phase voltages at 40Hz

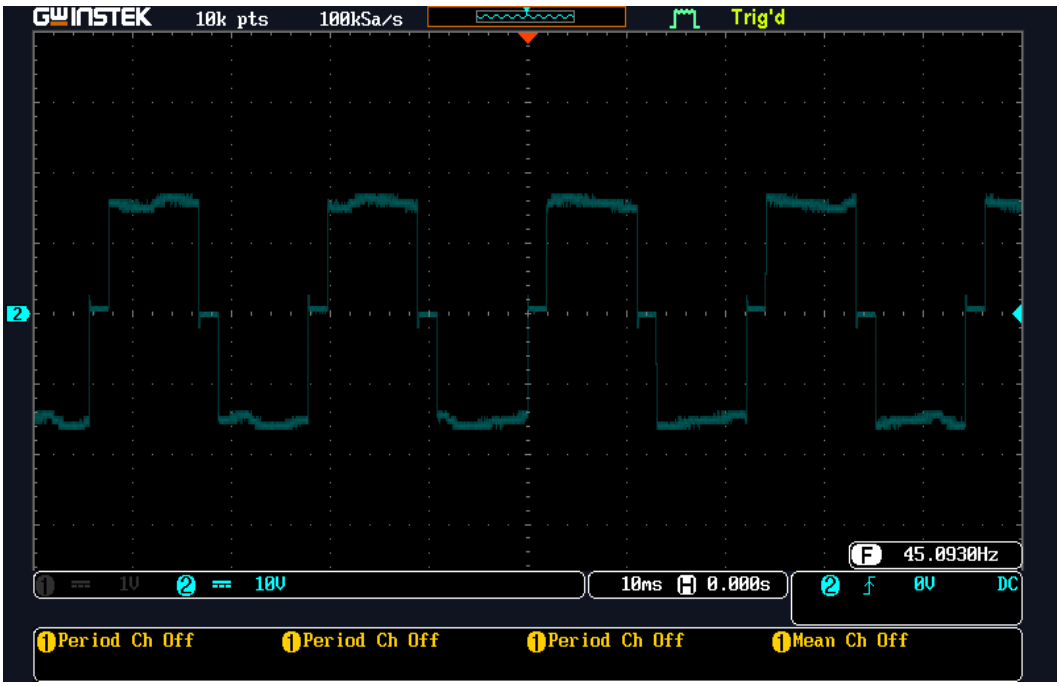


Fig. 7.9 : Experimental waveforms for phase to phase voltages at 45 Hz

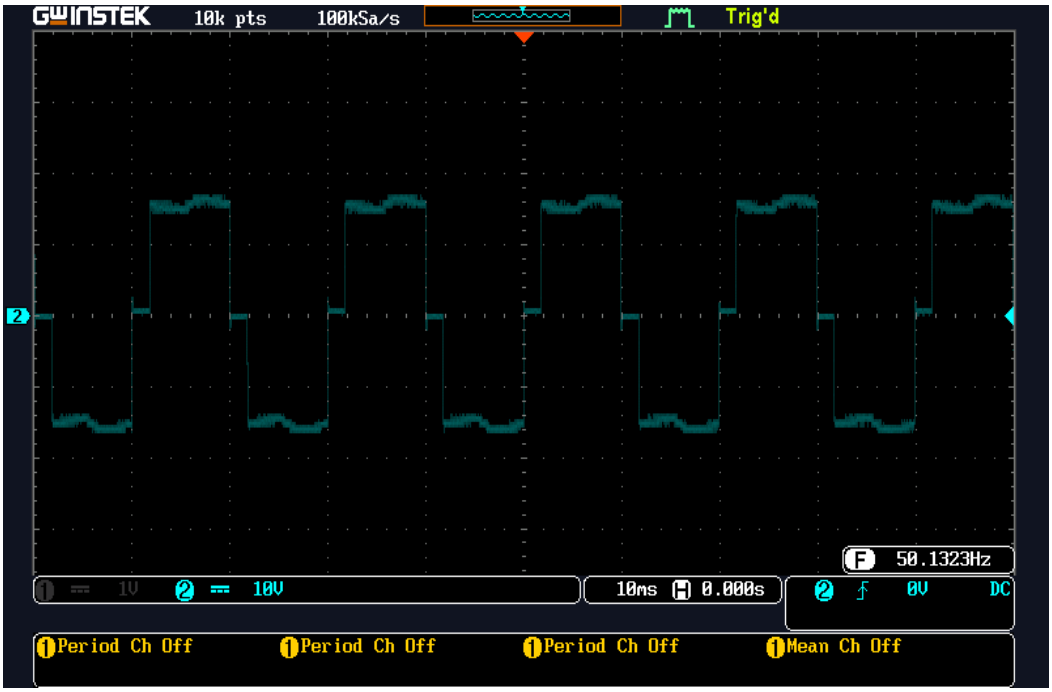


Fig. 7.10 : Experimental waveforms for phase to phase voltages at 50 Hz

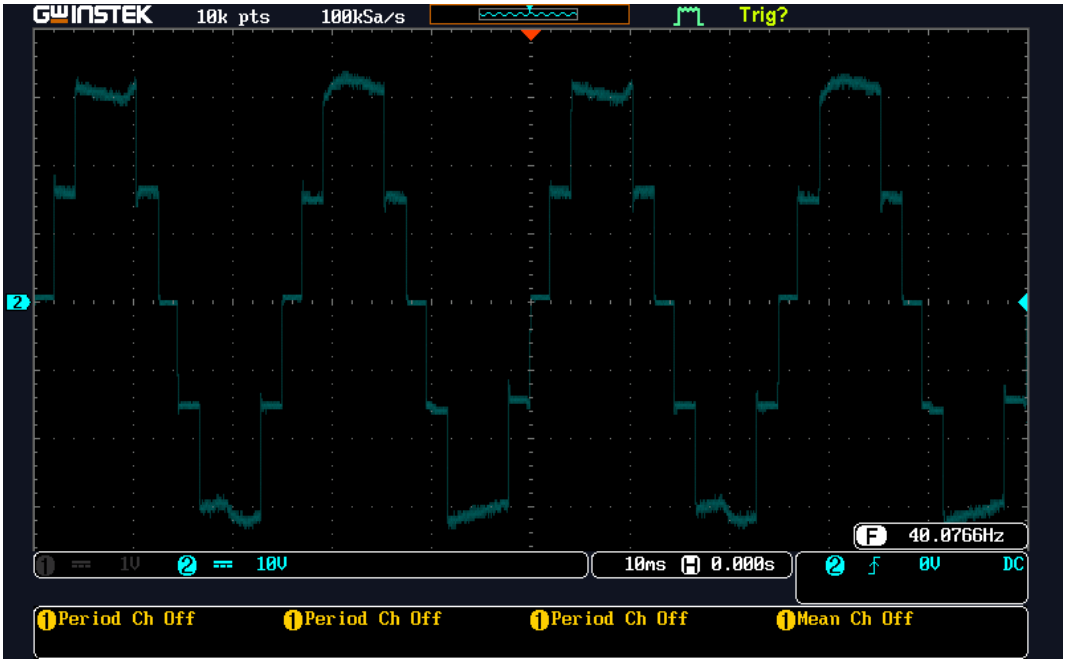


Fig. 7.11 : Experimental waveforms for line to line voltages at 40Hz

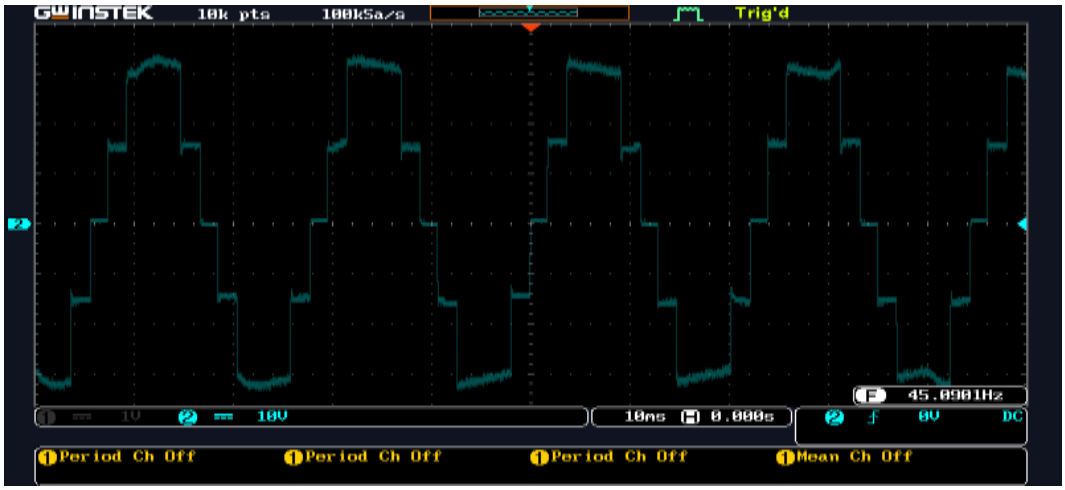


Fig. 7.12 : Experimental waveforms for line voltages at 45Hz

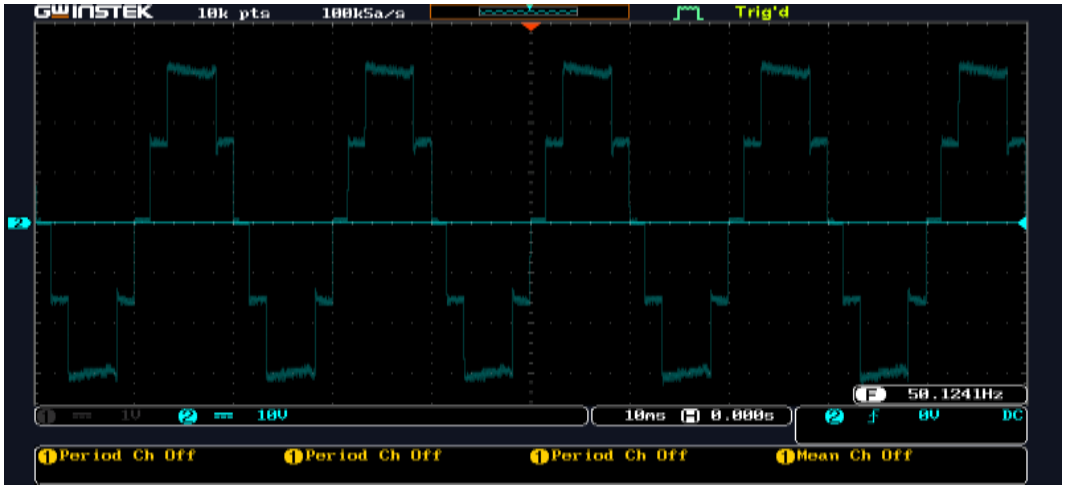


Fig. 7.13 : Experimental waveforms for lineto line voltages at 50Hz

Fig. 7.14 : Experimental waveforms for Inverter current

Table 7.4 : Variation in the speed of the motor as a function of load at 40 Hz

Sr. No.	Load (Kg)	Volt (V)	Current (A)	Load Power (W)	Torque (N-m)	Expected Speed (rpm)	Measured Speed (rpm)
1	0.5	260	1.23	320	2.48	1200	1240
2	1.0	260	1.26	330	2.56	1200	1240
3	1.5	260	1.30	340	2.64	1200	1240
4	2.0	260	1.34	350	2.71	1200	1240
5	2.5	260	1.38	360	2.79	1200	1240
6	3.0	260	1.42	370	2.87	1200	1240

Table 7.5 : Variation in the speed of the motor as a function of load at 45 Hz.

Sr. No.	Load (Kg)	Volt (V)	Current (A)	Power (W)	Torque (N-m)	Expected Speed (rpm)	Measured Speed (rpm)
1	0.5	264	1.13	300	2.08	1350	1380
2	1.0	264	1.13	300	2.08	1350	1380
3	1.5	264	1.17	310	2.15	1350	1380
4	2.0	264	1.21	320	2.22	1350	1380
5	2.5	264	1.25	330	2.29	1350	1380
6	3.0	264	1.25	330	2.29	1350	1380

Table 7.6 : Variation in the speed of the motor as a function of load at 50 Hz

Sr. No.	Load (Kg)	Volt (V)	Current (A)	Load Power (W)	Torque (N-m)	Expected Speed (rpm)	Measured Speed (rpm)
1	0.5	270	1.01	272	1.68	1500	1540
2	1.0	270	1.09	295	1.81	1500	1540
3	1.5	270	1.13	305	1.89	1500	1540
4	2.0	270	1.20	325	2.01	1500	1540
5	2.5	270	1.28	345	2.14	1500	1540
6	3.0	270	1.35	365	2.26	1500	1540

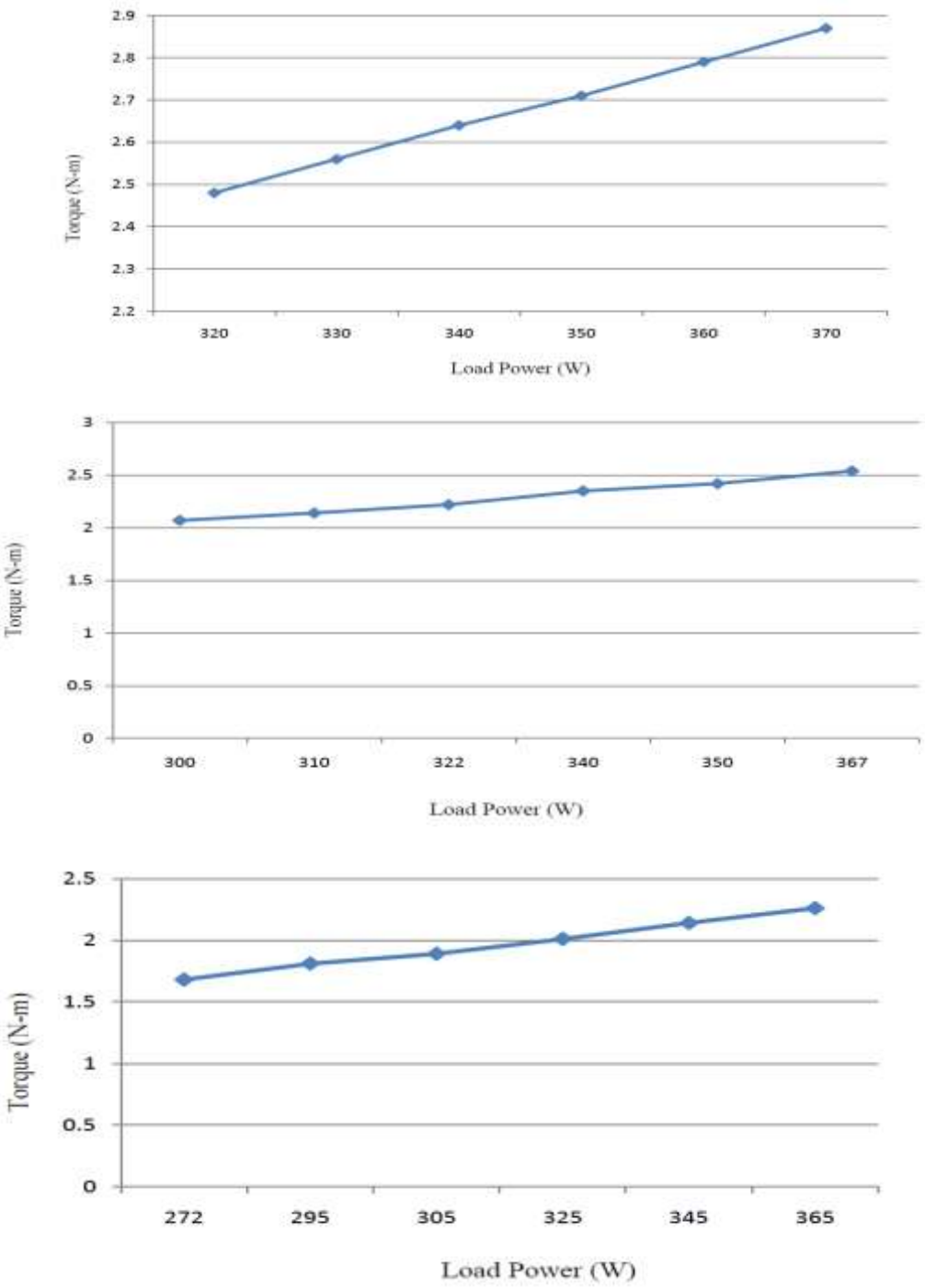


Fig. 7.15 : Torque Vs Load power Characteristics at 40 Hz, 45 Hz &50Hz

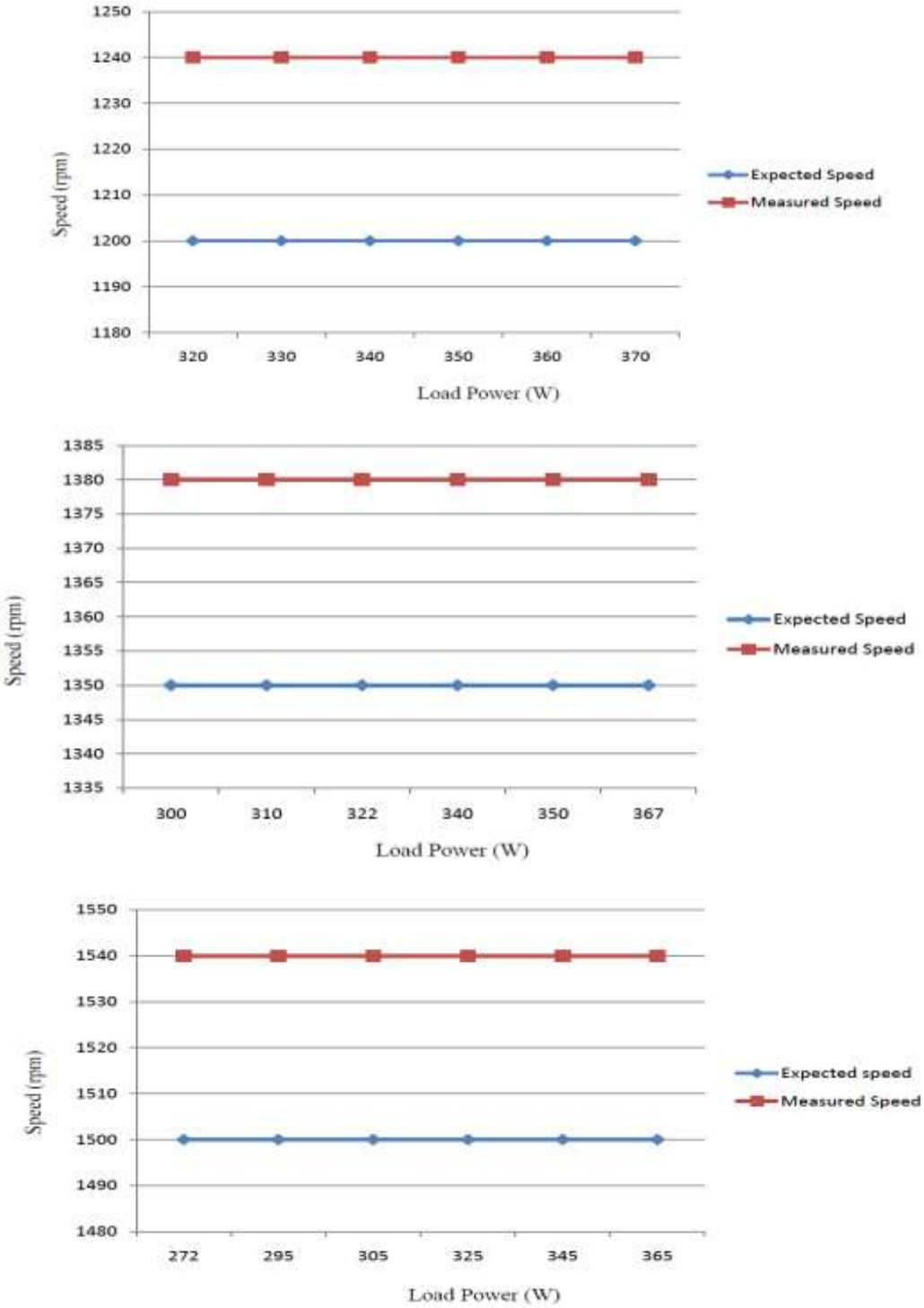


Fig. 7.16 : Speed Vs Load power Characteristics at 40 Hz, 45 Hz &50Hz

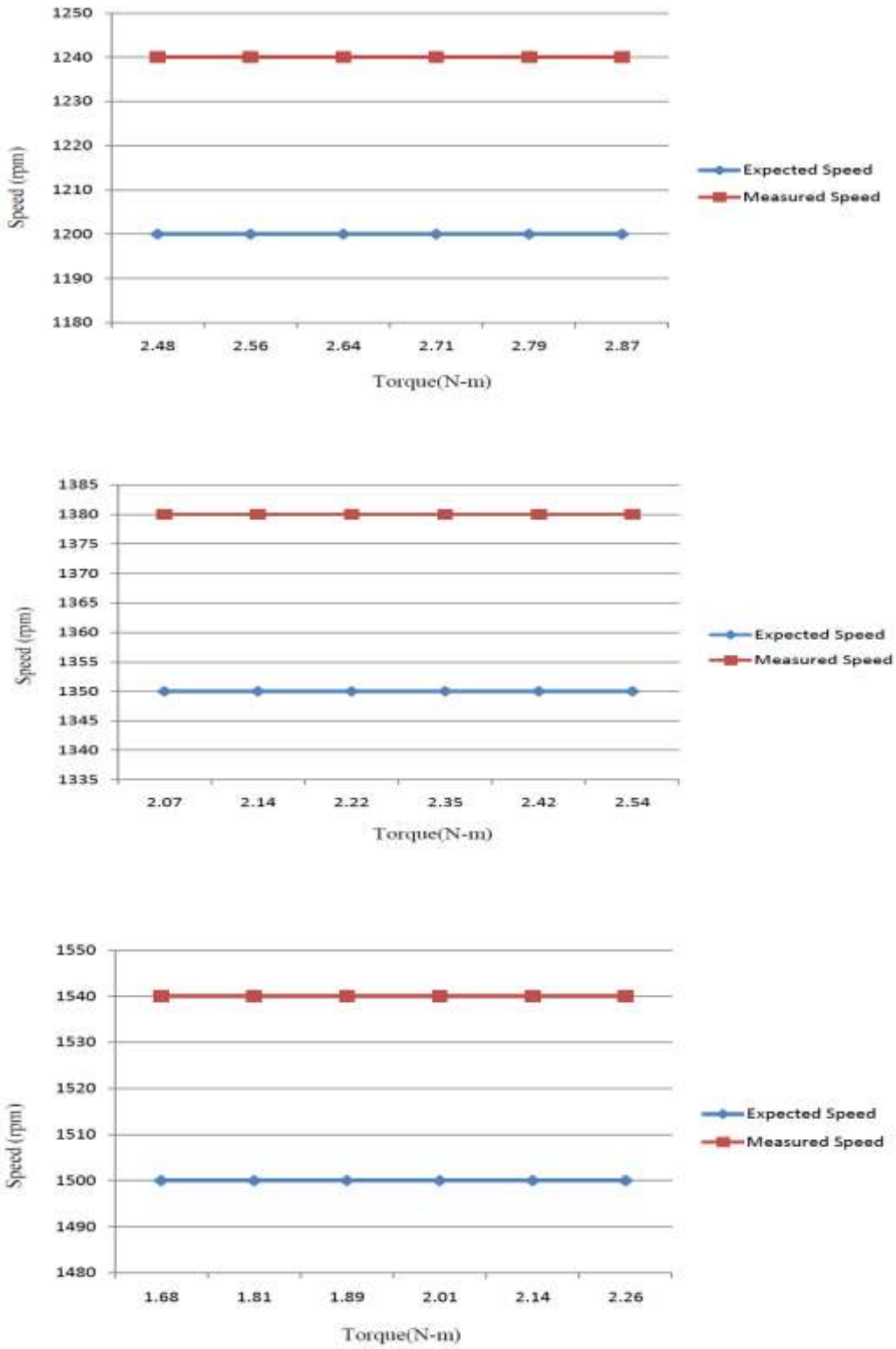


Fig. 7.17 : Speed Vs Torque Characteristics at 40 Hz, 45 Hz &50Hz

From the above observation and characteristics we conclude that, by varying the inverter frequency the speed of the motor also gets varied. If the frequency increases the speed of the motor also increases and if the frequency decreases the speed of the motor also decreases.

If the frequency is kept constant at particular value, the speed of the motor also remains constant, irrespective of the load.

7.6 CONCLUSION

An experimental setup was developed using an AVR Microcontroller. An experimental study is carried out with the aim of corroborating the effectiveness of the proposed AVR Microcontroller based CB-SVPWM control algorithms have been implemented and tested with a load of 3N.m. The DC link voltage is set to 380V. The speed performances are experimentally investigated for both techniques. Variation in the speed of the motor as a function of load at constant modulating frequency of 40 Hz, 45 Hz &50Hz are shown in table.7.4 to 7.6. Fig.7.15. to fig 7.17 shows Speed Vs Load Characteristics at Frequency 40 Hz, 45 Hz & 50Hz.

To verify the validity of the proposed CB- SVPWM scheme, a three–level diode clamped multilevel inverter (DCMLI) is designed to implement the scheme. Each phase of the main topology is a three–level diode clamped multilevel inverter (DCMLI) as shown in Fig.7.1 and the results are shown in Figs.7.9 to 7.13, where frequency of modulated wave and carrier wave are 50 Hz and 2.5 kHz, respectively. Fig.7.14 is output line current waves and its spectrum when CB-SVPWM is implemented, from the experiment results, the output voltage using CB-SVPWM scheme is evidently better than using SV-PWM scheme.

Chapter 8 talks about results analysis and discussion of FOC and DTC based three level diode clamped inverter fed PMSM drive under steady state & transient state condition, conclusions and future scope.

CHAPTER – 8

RESULTS ANALYSIS AND DISCUSSION

This chapter focuses on the results analysis and discussion of FOC &DTC based three level diode clamped inverter fed PMSM drive under steady state & transient state condition for automotive application.from the present research work conclusion have been clearly stated and the future work is also mentined.

8.1 SIMULATION RESULTS ANALYSIS

The simulation analysis of the FOC-CBSVPWM and DTC-CBSVPWM fed PMSM using three-level diode clamped IGBT inverter system is investigated. The control scheme applied for the electrical drive is field oriented control and direct torque control. The modulation techniques used is CBSVPWM. The system used, was investigated for steady and transient state response. The output waveforms of three phase voltage and current for three-level inverter and the torque speed response of three level diode-clamped inverter fed PMSM drive with DTC is estimated. The parameters used in this simulation are shown in below:

Ld=0.006365H;Lq=0.006365H; R=1.6Ω;PM_flux=0.1852Wb;P=2; F=0.00005396 Nm-s; J=0.0001854 Kgm^2

In this research work, the simulation model of FOC and DTC based closed loop control of three–level diode clamped multilevel inverter (DCMLI) fed PMSM drive using carrier based pulse width modulation(CB-SVPWM)techniques has studied. The output voltage, current of the inverter and the speed, torque and the three-phase currents of the PMSM for carrier based pulse width modulation (CB-SVPWM) techniques have plotted. Comparing the simulation results of the PMSM drive used in the electric vehicle under the control of the different control strategies, we can get conclusions as the following.

- In FOC-CBSVM, due to the lower sampling period, the stator current is more sinusoidal using the hysteresis current control. But it needs the continuous

rotor position information and the switching frequency of the three level diode clamped inverter is not constant. It causes torque and current ripples. In the FOC-CBSVM analysis, torque ripple percentage is15.38% .It is less as compared to FOC-PWM and FOC-SVPWM.

- In DTC- CBSVM, it does not need the rotor position information except for the initial rotor position. A novel carrier based space vector modulation technique using the switching table reduces current and torque ripples. Also maintained the switching frequency of the three level diode clamped inverter is constant. In the DTC-CBSVM analysis, torque ripple percentage is 10.52%. It is less as compared to FOC- CBSVM.
- From the analysis we can conclude that the DTC based three–level diode clamped multilevel inverter (DCMLI) fed PMSM drive gives better speed-torque characteristics compared to FOC based three–level diode clamped multilevel inverter (DCMLI) fed PMSM drive with less transients and good steady state response.
- The novel CBSVPWM is similar to SVPWM but much simple, easy and the fastest method without much mathematical calculations like angle and sector determination as in SVPWM. This method can be easily extended to n-level inverter. THD of voltage and current also reduces with CBSVPWM.
- The simulation results show that the proposed method can effectively suppress the torque ripple and improve driving performance for the PMSM drive in automotive application.
- From this analysis we can conclude that direct torque control using CBSVPWM for PMSM not only gives good dynamic performance but also reduces the total harmonic distortion of voltage and current as compared to field oriented control. Also CBSVPWM can be easily extended to n-level inverter without much complication.

8.2 HARDWARE RESULT ANALYSIS

An experimental setup was developed using a AVR Microcontroller. An experimental study is carried out with the aim of corroborating the effectiveness of the proposed AVR Microcontroller with a DTC based CB-SVPWM control algorithms have been implemented and tested with a load of 3N.m. From the experiment results, the output voltage using CB-SVPWM scheme is evidently better than using PWM scheme. A comparison of 3-level Diode clamped simulation and laboratory models has been carried out. Both models show that the results obtained corresponded to each others. The waveforms have the same shapes and values. The analyses have been conducted only for the 3-level Diode clamped inverter with a resistive load of 180 watts and a DC supply of 380V. The voltages obtained are 280V for line-to-line voltage and 160V for line-to-neutral voltage. The THD values of those three parameters, line-to-line voltage, VLL, line-to-neutral voltage and line current have been simulated.

8.3 CONCLUSIONS

- In this research work, the simulation model of field oriented control (F.O.C) and direct torque control(DTC) control of three-level diode clamped inverter fed PMSM drive using a novel carrier based space vector pulse width modulation (CBSVPWM) technique has been studied and implemented.
- DTC gives fast and dynamic performance as compare to FOC. A novel CB-SVM technique is similar to SVPWM but much simple, easy and the fastest method without many mathematical calculations like angle and sector determination. This method can be easily extended to n-level inverter. Therefore DTC-CBSVPWM gives simple, dynamic and fast response.
- The output voltage, current of the three-level diode clamped inverter and the speed, torque and the three-phase currents of PMSM have been plotted.
- The results are compared with the closed loop FOC. DTC-CBSVPWM gives better performance compared to conventional FOC.

- Hardware is designed and implemented for a three–level diode clamped multilevel inverter (DCMLI) fed PMSM drive using carrier based space vector modulation (CBSVPWM) based on AVR microcontroller.
- The three–level diode clamped multilevel inverter (DCMLI) fed PMSM drive is found acceptable because of its less distorted output, lower costs, better control performance and other advantageous features.
- Considering the better features of DTC-CBSVM over FOC. Hence A novel CB-SVM technique using three level diode clamped multilevel inverter has been proven to be a better choice.
- The simulation & hardware results show that the proposed method can effectively suppress the torque ripple and improve driving performance for the PMSM drive. Hence it is used in automotive application.

8.4 FUTURE SCOPE

The research work deals with three level diode clamped inverter used in PMSM.Many researchers design and implemented two level and three level inverters for the drives applications. However there is a ample scope to reduced the THD and torque ripples using n level inverters.

The current hardware will be extended to implement an five–level diode clamped multilevel inverter (DCMLI) fed PMSM drive using Carrier based space vector modulation (CBSVPWM) technique based of an AVR microcontroller. The classical Carrier based space vector modulation (CBSVPWM) method is used to generate the requested motor voltages. To improve the system performance in terms of torque ripple, power quality and better DC voltage utilization, Carrier based space vector modulation (CBSVPWM) can be employed for three –level diode clamped multilevel inverter (DCMLI) fed PMSM drive.

APPENDICES

A1- ROTOR AND STATOR OF PMSM MACHINE

A1.1. View of rotor (on the left side) and stator armature (on the right side) of PMSM.

A2 MICROPROCESSOR PROGRAMMING

A2.1 ATMEGA 8

```
/*
 * _3_level_3_phase.c
 *
 * Created: 06/07/2015 7:16:23 PM
 *  Author: a
 */



#include <avr/io.h>
#include <mega8.h>

#define Sa1_on cbi(PORTC,5);
#define Sa1_of sbi(PORTC,5);
#define Sa2_on cbi(PORTC,4);
#define Sa2_of sbi(PORTC,4);
#define Sa3_on cbi(PORTC,3);
#define Sa3_of sbi(PORTC,3);
#define Sa4_on cbi(PORTC,2);
#define Sa4_of sbi(PORTC,2);

#define Sb1_on cbi(PORTC,1);
#define Sb1_of sbi(PORTC,1);
#define Sb2_on cbi(PORTC,0);
#define Sb2_of sbi(PORTC,0);
#define Sb3_on cbi(PORTB,5);
#define Sb3_of sbi(PORTB,5);
#define Sb4_on cbi(PORTB,4);
#define Sb4_of sbi(PORTB,4);

#define Sc1_on cbi(PORTB,3);
```

```
#define Sc1_of sbi(PORTB,3);
#define Sc2_on cbi(PORTB,2);
#define Sc2_of sbi(PORTB,2);
#define Sc3_on cbi(PORTB,1);
#define Sc3_of sbi(PORTB,1);
#define Sc4_on cbi(PORTB,0);
#define Sc4_of sbi(PORTB,0);
void time(int x);
int main(void)
{
    PORTC|=0b111111;
    PORTB|=0b111111;
    DDRB|=0b111111;
    DDRC|=0b111111;
    PORTB|=0b111111;
    PORTC|=0b111111;
    DDRD=0b00001110;
    PORTD=0b11111111;
    int a=950;  //50Hz
   while(1)
   {
            if (bit_is_clear(PIND,7))
            {
                    a=1190;     //40Hz
                    cbi(PORTD,2);sbi(PORTD,3);sbi(PORTD,1);
            }
            if (bit_is_clear(PIND,6))
            {
                    a=1057;     //45Hz
                    cbi(PORTD,3);sbi(PORTD,2);sbi(PORTD,1);
            }
            if (bit_is_clear(PIND,5))
```

```
        {
                a=950;      //50Hz
                cbi(PORTD,1);sbi(PORTD,2);sbi(PORTD,3);
        }
        if (bit_is_clear(PIND,0))
        {
                if (a > 650)
                {
                        a=a-10;
                        _delay_ms(10);
                }
        }
        //Stage 1
Sa1_on;Sa2_on;Sa3_of;Sa4_of;      //1100
         Sb1_of;Sb2_of;Sb3_on;Sb4_on;       //0011
         Sc1_of;Sc2_of;Sc3_on;Sc4_on;       //0011
         time(a);Sb1_of;Sb2_of;Sb3_of;Sb4_of;_delay_us(5);
        //Stage 2
         Sa1_on;Sa2_on;Sa3_of;Sa4_of;       //1100
Sb1_of;Sb2_on;Sb3_on;Sb4_of;     //0110
Sc1_of;Sc2_of;Sc3_on;Sc4_on;      //0011
         time(a);Sb1_of;Sb2_of;Sb3_of;Sb4_of;_delay_us(5);
        //Stage 3
         Sa1_on;Sa2_on;Sa3_of;Sa4_of;       //1100
         Sb1_on;Sb2_on;Sb3_of;Sb4_of;   //1100
         Sc1_of;Sc2_of;Sc3_on;Sc4_on;       //0011
time(a);Sa1_of;Sa2_of;Sa3_of;Sa4_of;_delay_us(5);
        //stage 4
         Sa1_of;Sa2_on;Sa3_on;Sa4_of;       //0110
         Sb1_on;Sb2_on;Sb3_of;Sb4_of;   //1100
         Sc1_of;Sc2_of;Sc3_on;Sc4_on;       //0011
time(a);Sa1_of;Sa2_of;Sa3_of;Sa4_of;_delay_us(5);
```

```
//stage 5
 Sa1_of;Sa2_of;Sa3_on;Sa4_on;      //0011
 Sb1_on;Sb2_on;Sb3_of;Sb4_of;   //1100
 Sc1_of;Sc2_of;Sc3_on;Sc4_on;      //0011
 time(a);Sc1_of;Sc2_of;Sc3_of;Sc4_of;_delay_us(5);
//stage 6
 Sa1_of;Sa2_of;Sa3_on;Sa4_on;      //0011
 Sb1_on;Sb2_on;Sb3_of;Sb4_of;   //1100
 Sc1_of;Sc2_on;Sc3_on;Sc4_of;      //0110
 time(a);Sc1_of;Sc2_of;Sc3_of;Sc4_of;_delay_us(5);
//stage 7
 Sa1_of;Sa2_of;Sa3_on;Sa4_on;      //0011
 Sb1_on;Sb2_on;Sb3_of;Sb4_of;   //1100
 Sc1_on;Sc2_on;Sc3_of;Sc4_of;      //1100
        time(a);Sb1_of;Sb2_of;Sb3_of;Sb4_of;_delay_us(5);
//stage 8
 Sa1_of;Sa2_of;Sa3_on;Sa4_on;      //0011
 Sb1_of;Sb2_on;Sb3_on;Sb4_of;   //0110
 Sc1_on;Sc2_on;Sc3_of;Sc4_of;      //1100
        time(a);Sb1_of;Sb2_of;Sb3_of;Sb4_of;_delay_us(5);
       //stage 9
        Sa1_of;Sa2_of;Sa3_on;Sa4_on;       //0011
        Sb1_of;Sb2_of;Sb3_on;Sb4_on;   //0011
        Sc1_on;Sc2_on;Sc3_of;Sc4_of;       //1100
        time(a);Sa1_of;Sa2_of;Sa3_of;Sa4_of;_delay_us(5);
       //stage 10
        Sa1_of;Sa2_on;Sa3_on;Sa4_of;       //0110
        Sb1_of;Sb2_of;Sb3_on;Sb4_on;   //0011
        Sc1_on;Sc2_on;Sc3_of;Sc4_of;       //1100
        time(a);Sa1_of;Sa2_of;Sa3_of;Sa4_of;_delay_us(5);
       //stage 11
        Sa1_on;Sa2_on;Sa3_of;Sa4_of;       //1100
```

```
                Sb1_of;Sb2_of;Sb3_on;Sb4_on;   //0011
                Sc1_on;Sc2_on;Sc3_of;Sc4_of;       //1100
                time(a);Sc1_of;Sc2_of;Sc3_of;Sc4_of;_delay_us(5);
               //stage 12
                Sa1_on;Sa2_on;Sa3_of;Sa4_of;       //1100
                Sb1_of;Sb2_of;Sb3_on;Sb4_on;   //0011
                Sc1_of;Sc2_on;Sc3_on;Sc4_of;       //0110
                time(a);Sc1_of;Sc2_of;Sc3_of;Sc4_of;_delay_us(5);
    }
}
void time(int x)
{
    int i=0;
    while(x>=i)
    {
            i++;
            _delay_us(1);
    }
}
```

A2.2 ATMEGA 16

```
#include <mega16.h>

ISR(TIMER1_COMPA_vect);
unsigned int seconds = 0;

int main(void)
{
    PORTC=0x00;
    DDRC=0xFF;
    PORTC=0x00;
    DDRD=0b00010000;
    PORTD=0xFF;
    int i1=0;
    long startTime=0,counter=0,RPM=0,Rref=0,second=0;
    int state,prevState=0,sensor=0;
    long int
adc_v,v,V,V1,volt,adc_a,t=0,avg=0,u=0,c3=0,y=0,x=0,z=0,c1,c2,t1=0,t2=0,t3=0,t4=0
,t5=0,t6=0,j=0;
    float I,w,Pwr,Trq,sum,b;
    int E=0,l=0;
   Init_LCD();
    LCDClear();
    Init_Adc();
    TCCR1B = (1<<CS12)|(1<<WGM12)|(1<<CS10);
    OCR1A = 7;
    TIMSK |= 1<<OCIE1A;
    _delay_ms(200);
    sbi(PORTC,2);
    _delay_ms(1000);
    sbi(PORTC,1);
```

```
  _delay_ms(2000);
  sbi(PORTC,0);
  _delay_ms(1000);
  LCDWriteStringXY(11,0,"50Hz");
  sei();
 while(1)
 {
  /************** RPM COUNTER *************/
            counter=0;
            RPM=0;
            E=0;
            seconds=0;
  while(seconds < 3000)
  {
       sensor =  read_adc(0);
       if (sensor < 750)
       state = 1;
       else
       state = 0;
       if(state != prevState)
       {
                counter++;
                prevState = state;
       }
  }

  counter = counter / 2;
  RPM=counter*20;
    LCDWriteIntXY(0,0,RPM,4);
    LCDWriteStringXY(4,0,"R");

  /************** VOLTAGE MEARSURE *************/
```

```
  while(i1<=1500)
  {
        adc_v=read_adc(1);
        V=(312*adc_v);
        V1=V/1023;
        v=(v+V1);
        _delay_us(700);
        i1++;
  }
   volt=v/1501;
   LCDWriteIntXY(6,0,volt,3);
   LCDWriteStringXY(9,0,"V");
   v=0,volt=0,V1=0,adc_v=0,V=0;

/************** CURRENT MEARSURE ************/
 i1=0;
 sum=0.0;
 while(i1<=800)
 {
        adc_a=read_adc(2);
        b=adc_a/68.2;
        sum=sum+b;
        _delay_ms(1);
   i1++;
 }
        I=sum/801;
 sum=avg=u=w=y=z=0;
 i1=0;
/************** CURRENT MEARSURE ************/

  if (PIND==0b11111101)
```

```
{
        LCDWriteStringXY(11,0,"40Hz");
        Rref=1200;
}
if (PIND==0b11111011)
{
        LCDWriteStringXY(11,0,"45Hz");
        Rref=1350;
}
if (PIND==0b11110111)
{
        LCDWriteStringXY(11,0,"50Hz");
        Rref=1500;
}
if (PIND==0b11111110 && j==0)
{
        LCDWriteStringXY(11,0,"--Hz");
        cbi(PORTC,0);
        _delay_ms(700);
        cbi(PORTC,1);
        _delay_ms(500);
        cbi(PORTC,2);
        _delay_ms(500);
        j=1;
}
if(PIND==0b01111110 && j==1)
{
        LCDWriteStringXY(11,0,"--Hz");
        cbi(PORTC,2);
        _delay_ms(700);
        cbi(PORTC,1);
        _delay_ms(500);
```

```
                cbi(PORTC,0);
                _delay_ms(500);
                j=0;
        }

        E=Rref-RPM;
        if (E >= 90)
        {
                cbi(PORTD,4);
                _delay_ms(20);
                sbi(PORTD,4);
        }
    }
}

ISR(TIMER1_COMPA_vect)
{
    seconds++;

    if(seconds == 99000)
    {
            seconds = 0;
    }
}
```

A3 MOTOR PARAMETERS

Surface type motor

Power	P	0.5 H.P(373W)
Number of pole pairs	P	2
Phase current	I(rms)	1.5 A
Phase voltage	U(rms)	160V
Magnetic flux-linkage	ΨPM	0.1852Wb
Rotor speed	Ωm	1500rpm
Nominal torque	Me	4 N-m
Moment of the inertia	J	0.0001854 kgm^2
Stator winding resistance	Rs	1.6 Ω
Stator d-axis inductance	Ld	0.006365
Stator q-axis inductance	Lq	0.006365

A4 VOLTAGE SOURCE INVERTER PARAMETERS

Detailed date of IGBT transistors (module FAICHILD FGA15N120ANTDTU):

UCE =1200V, Ic = 15A

$VCEsat$ = 1.9 – 2.4 V, forward diode voltage 2.7V

Turn on time tr = 15ns, Fall time tf = 100ns

Delay of IGBT drivers tONd = 20ns T$OFFd$ =160 ns

T = tr + tONd = 35 ns total turn on time of IGBT

T = tf + t$OFFd$ = 260ns total turn off time of IGBT

Dead time Td =180 ns

PUBLICATIONS

Under Review at SCI Indexed Journals;

1. Mr.R.G.Shriwastava, Dr. M.B.Daigavane,Dr. S.R.Vaishnav, Dr. P.M.Daigavane, *"Simulation Analysis of FOC and DTC Based 3-Level DCMLI Fed PMSM Drive in Automotive Application"* is under review at SCI Indexed Canadian journal of Electrical and Computer Engineering.*(CJECE-OA-2015-Nov 255)*

2. Mr.R.G.Shriwastava, Dr. M.B.Daigavane,Dr. S.R.Vaishnav, Dr. P.M.Daigavane, *"Simulation and Experimental based Analysis of 3-level DCMLI Fed PMSM Drive using CBSVPWM"* is under review at SCI Indexed *Journal of Power Electronics(JPE-15-11-037)*

International Journals:

1. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. S. R. Vaishnav "*Application Characteristics of Permanent Magnet Synchronous Motors",* (Case Study) International Journal of Computer Information Systems (IJCIS)*Vol. 3, No. 3, 2011.*
2. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. S. R. Vaishnav *" Literature Review of Permanent Magnet AC Motors Drive for Automotive Application"*, Buletin Teknik Elektro dan Informatika (Bulletin of Electrical Engineering and Informatics) *Vol.1, No.1, March 2012, pp. 7~14*
3. Mr. R. G. Shriwastava, Dr. M. B.Daigavane, Dr. S. R. Vaishnav *"Torque Analysis of Permanent Magnet Synchronous Motor Used in Automotive Industry",* International joint journal of electrical &electronics engineering (IJJEE-2011)*Vol. 05, No. 02, Mar 2011(ACEEE DOI:01.IJRTET.05.02.85)*
4. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. S. R.Vaishnav *"Design Of A Permanent Magnet Synchronous Machine For The Electric Power Steering",* International Journal of Engineering Research and Applications (IJERA-2011) *Vol. 1, Issue 3, pp.646-653*
5. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. S. R. *Vaishnav " Intelligent control design of PMSM drive for Automotive Application",* International Journal of Scientific & Engineering Research(IJSER-2012) *Volume 3, Issue 5*
6. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. S. R. Vaishnav *"Design Of A Permanent Magnet Synchronous Machine For The Electric Power Steering",* International Journal of Advance Research in Electrical, Electronics and Instrumentation Engineering(IJAREEIE)*ISSN(print:2320-765ISSN(online):2278-8875Vol.3 Issus 3, March 2014.*

International Conferences:

1. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. S. R.Vaishnav. *"Electric power Steering with permanent magnet synchronous motor drive used in Automotive Application",* 1st International Conference on Electrical Energy System(ICEES-2011),03rdto 05rd January,2011 published in IEEExplore record no *978-1-61284-379.2011;* 145-148
2. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. S. R. Vaishnav*"Electric Design and Simulation of PMSM Drive for EPS Applications using MATLAB"*,3rd International Conference on Circuits,Power and Computing Technologies(ICCPCT-2013),20thto 22th March,2013 published in IEEExplore Conference record no10.1109/ICCPCT.2013.6528942.6528942.213; 152-159
3. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. S. R. Vaishnav, "*Sensorless Field oriented control of PMSM Drive System for Automotive Application*" , 7th International Conference on Emerging Trends in Engineering and Technology, 18th to 20th November,2015, Kobe Japan. (published in IEEExplore)

Under Review at International Conferences:

1. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. P. M. Daigavane, "*Simulation Analysis of 3-level Diode Clamped Multilevel Inverter Fed PMSM Drive using carrier based space vector Pulse Width Modulation (CP-SVPWM)", in 7th Annual International Conference, ICCCV 2016 in Association with Elsevier Publication during Feb 26-27, 2016.*

2. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. P. M. Daigavane, *"Simulation & Experimental Verification of DCMLI Using SVPWM based on a AVR Microcontroller" in 6th IEEE International Conference on Power Systems (ICPS 2016) at Indian Institute of Technology Delhi during March 4-6, 2016."*

3. Mr. R. G. Shriwastava, Dr. M. B. Daigavane, Dr. P. M. Daigavane, *"A Simulation Analysis of Matrix Converter Fed PMSM drive system". in INDIACOM-2016 during March 16-18, 2016*

National Conference:

1. Mr.R.G.Shriwastava, Dr. M.B.Daigavane,Dr. S.R.Vaishnav, "Simulation of VSI Fed Variable Speed Permanent Magnet Synchronous Motor Drive for Automotive Application", 3rd National Conference on "Power Electronics and Intelligent control", 1.11.2012 to 2.11.2012 at Malviya National Institute of Technology, Jaipur.

Datasheets:

FAIRCHILD SEMICONDUCTOR®

November 2013

FGA15N120ANTDTU

1200 V, 15 A NPT Trench IGBT

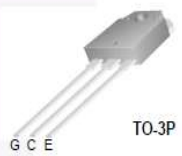
Features

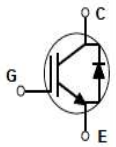
- NPT Trench Technology, Positive temperature coefficient
- Low Saturation Voltage: $V_{CE(sat), typ}$ = 1.9 V @ I_C = 15 A and T_C = 25°C
- Low Switching Loss: $E_{off, typ}$ = 0.6 mJ @ I_C = 15 A and T_C = 25°C
- Extremely Enhanced Avalanche Capability

Description

Using Fairchild's proprietary trench design and advanced NPT technology, the 1200V NPT IGBT offers superior conduction and switching performances, high avalanche ruggedness and easy parallel operation.

This device is well suited for the resonant or soft switching application such as induction heating, microwave oven.





Absolute Maximum Ratings

Symbol	Description		Ratings	Unit
V_{CES}	Collector-Emitter Voltage		1200	V
V_{GES}	Gate-Emitter Voltage		± 20	V
I_C	Collector Current	@ T_C = 25°C	30	A
	Collector Current	@ T_C = 100°C	15	A
I_{CM}	Pulsed Collector Current (Note 1)		45	A
I_F	Diode Continuous Forward Current	@ T_C = 25°C	30	A
	Diode Continuous Forward Current	@ T_C = 100°C	15	A
I_{FM}	Diode Maximum Forward Current		45	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	186	W
	Maximum Power Dissipation	@ T_C = 100°C	74	W
T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for IGBT	--	0.67	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for Diode	--	2.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Notes:
(1) Repetitive rating: Pulse width limited by max. junction temperature

FGA15N120ANTDTU — 1200 V, 15 A NPT Trench IGBT

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FGA15N120ANTDTU_F109	FGA15N120ANTDTU	TO-3P	Tube	N/A	N/A	30

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
I_{CES}	Collector Cut-Off Current	$V_{CE} = V_{CES}$, V_{GE} = 0 V	--	--	3	mA
I_{GES}	G-E Leakage Current	$V_{GE} = V_{GES}$, V_{CE} = 0 V	--	--	± 250	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 15 mA, $V_{CE} = V_{GE}$	4.5	6.5	8.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 15 A, V_{GE} = 15 V	--	1.9	2.4	V
		I_C = 15 A, V_{GE} = 15 V, T_C = 125°C	--	2.2	--	V
		I_C = 30 A, V_{GE} = 15 V	--	2.3	--	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30 V, V_{GE} = 0 V, f = 1 MHz	--	2650	--	pF
C_{oes}	Output Capacitance		--	143	--	pF
C_{res}	Reverse Transfer Capacitance		--	96	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 25°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	--	ns
t_f	Fall Time		--	100	180	ns
E_{on}	Turn-On Switching Loss		--	3	4.5	mJ
E_{off}	Turn-Off Switching Loss		--	0.6	0.9	mJ
E_{ts}	Total Switching Loss		--	3.6	5.4	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 125°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	170	--	ns
t_f	Fall Time		--	150	--	ns
E_{on}	Turn-On Switching Loss		--	3.2	4.8	mJ
E_{off}	Turn-Off Switching Loss		--	0.8	1.2	mJ
E_{ts}	Total Switching Loss		--	4.0	6.0	mJ
Q_g	Total Gate Charge	V_{CE} = 600 V, I_C = 15 A, V_{GE} = 15 V	--	120	180	nC
Q_{ge}	Gate-Emitter Charge		--	16	22	nC
Q_{gc}	Gate-Collector Charge		--	50	65	nC

Electrical Characteristics of DIODE T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{FM}	Diode Forward Voltage	I_F = 15 A	T_C = 25°C	–	1.7	2.7	V
			T_C = 125°C	–	1.8	–	
t_{rr}	Diode Reverse Recovery Time	I_F = 15 A di_F/dt = 200 A/µs	T_C = 25°C	–	210	330	ns
			T_C = 125°C	–	280	–	
I_{rr}	Diode Peak Reverse Recovery Current		T_C = 25°C	–	27	40	A
			T_C = 125°C	–	31	–	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	–	2835	6600	nC
			T_C = 125°C	–	4340	–	

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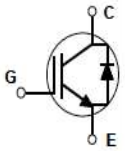

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I_{FM}	Diode Maximum Forward Current		45	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	186	W
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T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for IGBT	--	0.67	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for Diode	--	2.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Notes:
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Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
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I_{GES}	G-E Leakage Current	$V_{GE} = V_{GES}$, V_{CE} = 0 V	--	--	± 250	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 15 mA, $V_{CE} = V_{GE}$	4.5	6.5	8.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 15 A, V_{GE} = 15 V	--	1.9	2.4	V
		I_C = 15 A, V_{GE} = 15 V, T_C = 125°C	--	2.2	--	V
		I_C = 30 A, V_{GE} = 15 V	--	2.3	--	V
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C_{ies}	Input Capacitance	V_{CE} = 30 V, V_{GE} = 0 V, f = 1 MHz	--	2650	--	pF
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$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 25°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	--	ns
t_f	Fall Time		--	100	180	ns
E_{on}	Turn-On Switching Loss		--	3	4.5	mJ
E_{off}	Turn-Off Switching Loss		--	0.6	0.9	mJ
E_{ts}	Total Switching Loss		--	3.6	5.4	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 125°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	170	--	ns
t_f	Fall Time		--	150	--	ns
E_{on}	Turn-On Switching Loss		--	3.2	4.8	mJ
E_{off}	Turn-Off Switching Loss		--	0.8	1.2	mJ
E_{ts}	Total Switching Loss		--	4.0	6.0	mJ
Q_g	Total Gate Charge	V_{CE} = 600 V, I_C = 15 A, V_{GE} = 15 V	--	120	180	nC
Q_{ge}	Gate-Emitter Charge		--	16	22	nC
Q_{gc}	Gate-Collector Charge		--	50	65	nC

Electrical Characteristics of DIODE T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{FM}	Diode Forward Voltage	I_F = 15 A	T_C = 25°C	–	1.7	2.7	V
			T_C = 125°C	–	1.8	–	
t_{rr}	Diode Reverse Recovery Time	I_F = 15 A di_F/dt = 200 A/µs	T_C = 25°C	–	210	330	ns
			T_C = 125°C	–	280	–	
I_{rr}	Diode Peak Reverse Recovery Current		T_C = 25°C	–	27	40	A
			T_C = 125°C	–	31	–	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	–	2835	6600	nC
			T_C = 125°C	–	4340	–	

FAIRCHILD SEMICONDUCTOR®

November 2013

FGA15N120ANTDTU

1200 V, 15 A NPT Trench IGBT

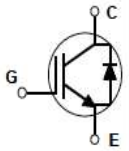
Features

- NPT Trench Technology, Positive temperature coefficient
- Low Saturation Voltage: $V_{CE(sat), typ}$ = 1.9 V @ I_C = 15 A and T_C = 25°C
- Low Switching Loss: $E_{off, typ}$ = 0.6 mJ @ I_C = 15 A and T_C = 25°C
- Extremely Enhanced Avalanche Capability

Description

Using Fairchild's proprietary trench design and advanced NPT technology, the 1200V NPT IGBT offers superior conduction and switching performances, high avalanche ruggedness and easy parallel operation.

This device is well suited for the resonant or soft switching application such as induction heating, microwave oven.



Absolute Maximum Ratings

Symbol	Description		Ratings	Unit
V_{CES}	Collector-Emitter Voltage		1200	V
V_{GES}	Gate-Emitter Voltage		± 20	V
I_C	Collector Current	@ T_C = 25°C	30	A
	Collector Current	@ T_C = 100°C	15	A
I_{CM}	Pulsed Collector Current (Note 1)		45	A
I_F	Diode Continuous Forward Current	@ T_C = 25°C	30	A
	Diode Continuous Forward Current	@ T_C = 100°C	15	A
I_{FM}	Diode Maximum Forward Current		45	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	186	W
	Maximum Power Dissipation	@ T_C = 100°C	74	W
T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for IGBT	--	0.67	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for Diode	--	2.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Notes:
(1) Repetitive rating: Pulse width limited by max. junction temperature

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FGA15N120ANTDTU_F109	FGA15N120ANTDTU	TO-3P	Tube	N/A	N/A	30

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
I_{CES}	Collector Cut-Off Current	$V_{CE} = V_{CES}$, V_{GE} = 0 V	--	--	3	mA
I_{GES}	G-E Leakage Current	$V_{GE} = V_{GES}$, V_{CE} = 0 V	--	--	± 250	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 15 mA, $V_{CE} = V_{GE}$	4.5	6.5	8.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 15 A, V_{GE} = 15 V	--	1.9	2.4	V
		I_C = 15 A, V_{GE} = 15 V, T_C = 125°C	--	2.2	--	V
		I_C = 30 A, V_{GE} = 15 V	--	2.3	--	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30 V, V_{GE} = 0 V, f = 1 MHz	--	2650	--	pF
C_{oes}	Output Capacitance		--	143	--	pF
C_{res}	Reverse Transfer Capacitance		--	96	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 25°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	--	ns
t_f	Fall Time		--	100	180	ns
E_{on}	Turn-On Switching Loss		--	3	4.5	mJ
E_{off}	Turn-Off Switching Loss		--	0.6	0.9	mJ
E_{ts}	Total Switching Loss		--	3.6	5.4	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 125°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	170	--	ns
t_f	Fall Time		--	150	--	ns
E_{on}	Turn-On Switching Loss		--	3.2	4.8	mJ
E_{off}	Turn-Off Switching Loss		--	0.8	1.2	mJ
E_{ts}	Total Switching Loss		--	4.0	6.0	mJ
Q_g	Total Gate Charge	V_{CE} = 600 V, I_C = 15 A, V_{GE} = 15 V	--	120	180	nC
Q_{ge}	Gate-Emitter Charge		--	16	22	nC
Q_{gc}	Gate-Collector Charge		--	50	65	nC

Electrical Characteristics of DIODE T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{FM}	Diode Forward Voltage	I_F = 15 A	T_C = 25°C	–	1.7	2.7	V
			T_C = 125°C	–	1.8	–	
t_{rr}	Diode Reverse Recovery Time	I_F = 15 A di_F/dt = 200 A/µs	T_C = 25°C	–	210	330	ns
			T_C = 125°C	–	280	–	
I_{rr}	Diode Peak Reverse Recovery Current		T_C = 25°C	–	27	40	A
			T_C = 125°C	–	31	–	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	–	2835	6600	nC
			T_C = 125°C	–	4340	–	

FAIRCHILD SEMICONDUCTOR®

November 2013

FGA15N120ANTDTU

1200 V, 15 A NPT Trench IGBT

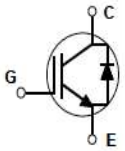
Features

- NPT Trench Technology, Positive temperature coefficient
- Low Saturation Voltage: $V_{CE(sat), typ}$ = 1.9 V @ I_C = 15 A and T_C = 25°C
- Low Switching Loss: $E_{off, typ}$ = 0.6 mJ @ I_C = 15 A and T_C = 25°C
- Extremely Enhanced Avalanche Capability

Description

Using Fairchild's proprietary trench design and advanced NPT technology, the 1200V NPT IGBT offers superior conduction and switching performances, high avalanche ruggedness and easy parallel operation.

This device is well suited for the resonant or soft switching application such as induction heating, microwave oven.



Absolute Maximum Ratings

Symbol	Description		Ratings	Unit
V_{CES}	Collector-Emitter Voltage		1200	V
V_{GES}	Gate-Emitter Voltage		± 20	V
I_C	Collector Current	@ T_C = 25°C	30	A
	Collector Current	@ T_C = 100°C	15	A
I_{CM}	Pulsed Collector Current (Note 1)		45	A
I_F	Diode Continuous Forward Current	@ T_C = 25°C	30	A
	Diode Continuous Forward Current	@ T_C = 100°C	15	A
I_{FM}	Diode Maximum Forward Current		45	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	186	W
	Maximum Power Dissipation	@ T_C = 100°C	74	W
T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for IGBT	--	0.67	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for Diode	--	2.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Notes:
(1) Repetitive rating: Pulse width limited by max. junction temperature

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FGA15N120ANTDTU_F109	FGA15N120ANTDTU	TO-3P	Tube	N/A	N/A	30

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
I_{CES}	Collector Cut-Off Current	$V_{CE} = V_{CES}$, V_{GE} = 0 V	--	--	3	mA
I_{GES}	G-E Leakage Current	$V_{GE} = V_{GES}$, V_{CE} = 0 V	--	--	± 250	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 15 mA, $V_{CE} = V_{GE}$	4.5	6.5	8.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 15 A, V_{GE} = 15 V	--	1.9	2.4	V
		I_C = 15 A, V_{GE} = 15 V, T_C = 125°C	--	2.2	--	V
		I_C = 30 A, V_{GE} = 15 V	--	2.3	--	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30 V, V_{GE} = 0 V, f = 1 MHz	--	2650	--	pF
C_{oes}	Output Capacitance		--	143	--	pF
C_{res}	Reverse Transfer Capacitance		--	96	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 25°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	--	ns
t_f	Fall Time		--	100	180	ns
E_{on}	Turn-On Switching Loss		--	3	4.5	mJ
E_{off}	Turn-Off Switching Loss		--	0.6	0.9	mJ
E_{ts}	Total Switching Loss		--	3.6	5.4	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 125°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	170	--	ns
t_f	Fall Time		--	150	--	ns
E_{on}	Turn-On Switching Loss		--	3.2	4.8	mJ
E_{off}	Turn-Off Switching Loss		--	0.8	1.2	mJ
E_{ts}	Total Switching Loss		--	4.0	6.0	mJ
Q_g	Total Gate Charge	V_{CE} = 600 V, I_C = 15 A, V_{GE} = 15 V	--	120	180	nC
Q_{ge}	Gate-Emitter Charge		--	16	22	nC
Q_{gc}	Gate-Collector Charge		--	50	65	nC

Electrical Characteristics of DIODE T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{FM}	Diode Forward Voltage	I_F = 15 A	T_C = 25°C	–	1.7	2.7	V
			T_C = 125°C	–	1.8	–	
t_{rr}	Diode Reverse Recovery Time	I_F = 15 A di_F/dt = 200 A/µs	T_C = 25°C	–	210	330	ns
			T_C = 125°C	–	280	–	
I_{rr}	Diode Peak Reverse Recovery Current		T_C = 25°C	–	27	40	A
			T_C = 125°C	–	31	–	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	–	2835	6600	nC
			T_C = 125°C	–	4340	–	

FAIRCHILD SEMICONDUCTOR®

November 2013

FGA15N120ANTDTU

1200 V, 15 A NPT Trench IGBT

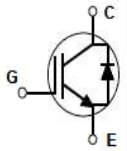
Features

- NPT Trench Technology, Positive temperature coefficient
- Low Saturation Voltage: $V_{CE(sat), typ}$ = 1.9 V @ I_C = 15 A and T_C = 25°C
- Low Switching Loss: $E_{off, typ}$ = 0.6 mJ @ I_C = 15 A and T_C = 25°C
- Extremely Enhanced Avalanche Capability

Description

Using Fairchild's proprietary trench design and advanced NPT technology, the 1200V NPT IGBT offers superior conduction and switching performances, high avalanche ruggedness and easy parallel operation.

This device is well suited for the resonant or soft switching application such as induction heating, microwave oven.



Absolute Maximum Ratings

Symbol	Description		Ratings	Unit
V_{CES}	Collector-Emitter Voltage		1200	V
V_{GES}	Gate-Emitter Voltage		± 20	V
I_C	Collector Current	@ T_C = 25°C	30	A
	Collector Current	@ T_C = 100°C	15	A
I_{CM}	Pulsed Collector Current (Note 1)		45	A
I_F	Diode Continuous Forward Current	@ T_C = 25°C	30	A
	Diode Continuous Forward Current	@ T_C = 100°C	15	A
I_{FM}	Diode Maximum Forward Current		45	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	186	W
	Maximum Power Dissipation	@ T_C = 100°C	74	W
T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for IGBT	--	0.67	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for Diode	--	2.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Notes:
(1) Repetitive rating: Pulse width limited by max. junction temperature

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FGA15N120ANTDTU_F109	FGA15N120ANTDTU	TO-3P	Tube	N/A	N/A	30

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
I_{CES}	Collector Cut-Off Current	$V_{CE} = V_{CES}$, V_{GE} = 0 V	--	--	3	mA
I_{GES}	G-E Leakage Current	$V_{GE} = V_{GES}$, V_{CE} = 0 V	--	--	± 250	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 15 mA, $V_{CE} = V_{GE}$	4.5	6.5	8.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 15 A, V_{GE} = 15 V	--	1.9	2.4	V
		I_C = 15 A, V_{GE} = 15 V, T_C = 125°C	--	2.2	--	V
		I_C = 30 A, V_{GE} = 15 V	--	2.3	--	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30 V, V_{GE} = 0 V, f = 1 MHz	--	2650	--	pF
C_{oes}	Output Capacitance		--	143	--	pF
C_{res}	Reverse Transfer Capacitance		--	96	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 25°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	--	ns
t_f	Fall Time		--	100	180	ns
E_{on}	Turn-On Switching Loss		--	3	4.5	mJ
E_{off}	Turn-Off Switching Loss		--	0.6	0.9	mJ
E_{ts}	Total Switching Loss		--	3.6	5.4	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 125°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	170	--	ns
t_f	Fall Time		--	150	--	ns
E_{on}	Turn-On Switching Loss		--	3.2	4.8	mJ
E_{off}	Turn-Off Switching Loss		--	0.8	1.2	mJ
E_{ts}	Total Switching Loss		--	4.0	6.0	mJ
Q_g	Total Gate Charge	V_{CE} = 600 V, I_C = 15 A, V_{GE} = 15 V	--	120	180	nC
Q_{ge}	Gate-Emitter Charge		--	16	22	nC
Q_{gc}	Gate-Collector Charge		--	50	65	nC

Electrical Characteristics of DIODE T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{FM}	Diode Forward Voltage	I_F = 15 A	T_C = 25°C	–	1.7	2.7	V
			T_C = 125°C	–	1.8	–	
t_{rr}	Diode Reverse Recovery Time	I_F = 15 A di_F/dt = 200 A/µs	T_C = 25°C	–	210	330	ns
			T_C = 125°C	–	280	–	
I_{rr}	Diode Peak Reverse Recovery Current		T_C = 25°C	–	27	40	A
			T_C = 125°C	–	31	–	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	–	2835	6600	nC
			T_C = 125°C	–	4340	–	

FAIRCHILD SEMICONDUCTOR®

November 2013

FGA15N120ANTDTU

1200 V, 15 A NPT Trench IGBT

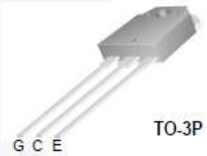
Features

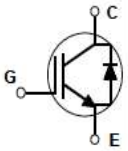
- NPT Trench Technology, Positive temperature coefficient
- Low Saturation Voltage: $V_{CE(sat), typ}$ = 1.9 V @ I_C = 15 A and T_C = 25°C
- Low Switching Loss: $E_{off, typ}$ = 0.6 mJ @ I_C = 15 A and T_C = 25°C
- Extremely Enhanced Avalanche Capability

Description

Using Fairchild's proprietary trench design and advanced NPT technology, the 1200V NPT IGBT offers superior conduction and switching performances, high avalanche ruggedness and easy parallel operation.

This device is well suited for the resonant or soft switching application such as induction heating, microwave oven.





Absolute Maximum Ratings

Symbol	Description		Ratings	Unit
V_{CES}	Collector-Emitter Voltage		1200	V
V_{GES}	Gate-Emitter Voltage		± 20	V
I_C	Collector Current	@ T_C = 25°C	30	A
	Collector Current	@ T_C = 100°C	15	A
I_{CM}	Pulsed Collector Current (Note 1)		45	A
I_F	Diode Continuous Forward Current	@ T_C = 25°C	30	A
	Diode Continuous Forward Current	@ T_C = 100°C	15	A
I_{FM}	Diode Maximum Forward Current		45	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	186	W
	Maximum Power Dissipation	@ T_C = 100°C	74	W
T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for IGBT	--	0.67	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case for Diode	--	2.88	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Notes:

(1) Repetitive rating: Pulse width limited by max. junction temperature

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FGA15N120ANTDTU_F109	FGA15N120ANTDTU	TO-3P	Tube	N/A	N/A	30

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
I_{CES}	Collector Cut-Off Current	$V_{CE} = V_{CES}$, V_{GE} = 0 V	--	--	3	mA
I_{GES}	G-E Leakage Current	$V_{GE} = V_{GES}$, V_{CE} = 0 V	--	--	± 250	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 15 mA, $V_{CE} = V_{GE}$	4.5	6.5	8.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 15 A, V_{GE} = 15 V	--	1.9	2.4	V
		I_C = 15 A, V_{GE} = 15 V, T_C = 125°C	--	2.2	--	V
		I_C = 30 A, V_{GE} = 15 V	--	2.3	--	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30 V, V_{GE} = 0 V, f = 1 MHz	--	2650	--	pF
C_{oes}	Output Capacitance		--	143	--	pF
C_{res}	Reverse Transfer Capacitance		--	96	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 25°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	160	--	ns
t_f	Fall Time		--	100	180	ns
E_{on}	Turn-On Switching Loss		--	3	4.5	mJ
E_{off}	Turn-Off Switching Loss		--	0.6	0.9	mJ
E_{ts}	Total Switching Loss		--	3.6	5.4	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 600 V, I_C = 15 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 125°C	--	15	--	ns
t_r	Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	170	--	ns
t_f	Fall Time		--	150	--	ns
E_{on}	Turn-On Switching Loss		--	3.2	4.8	mJ
E_{off}	Turn-Off Switching Loss		--	0.8	1.2	mJ
E_{ts}	Total Switching Loss		--	4.0	6.0	mJ
Q_g	Total Gate Charge	V_{CE} = 600 V, I_C = 15 A, V_{GE} = 15 V	--	120	180	nC
Q_{ge}	Gate-Emitter Charge		--	16	22	nC
Q_{gc}	Gate-Collector Charge		--	50	65	nC

Electrical Characteristics of DIODE T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{FM}	Diode Forward Voltage	I_F = 15 A	T_C = 25°C	–	1.7	2.7	V
			T_C = 125°C	–	1.8	–	
t_{rr}	Diode Reverse Recovery Time	I_F = 15 A di_F/dt = 200 A/µs	T_C = 25°C	–	210	330	ns
			T_C = 125°C	–	280	–	
I_{rr}	Diode Peak Reverse Recovery Current		T_C = 25°C	–	27	40	A
			T_C = 125°C	–	31	–	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	–	2835	6600	nC
			T_C = 125°C	–	4340	–	

Features

- High-performance, Low-power Atmel®AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 × 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16MIPS Throughput at 16MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 8Kbytes of In-System Self-programmable Flash program memory
  - 512Bytes EEPROM
  - 1Kbyte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[1]
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler, one Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Three PWM Channels
  - 8-channel ADC in TQFP and QFN/MLF package
    Eight Channels 10-bit Accuracy
  - 6-channel ADC in PDIP package
    Six Channels 10-bit Accuracy
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-lead PDIP, 32-lead TQFP, and 32-pad QFN/MLF
- Operating Voltages
  - 2.7V - 5.5V (ATmega8L)
  - 4.5V - 5.5V (ATmega8)
- Speed Grades
  - 0 - 8MHz (ATmega8L)
  - 0 - 16MHz (ATmega8)
- Power Consumption at 4Mhz, 3V, 25°C
  - Active: 3.6mA
  - Idle Mode: 1.0mA
  - Power-down Mode: 0.5µA

Atmel

8-bit Atmel with 8KBytes In-System Programmable Flash

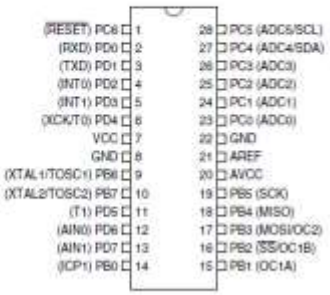
ATmega8
ATmega8L

Rev.2486AA–AVR–02/2013

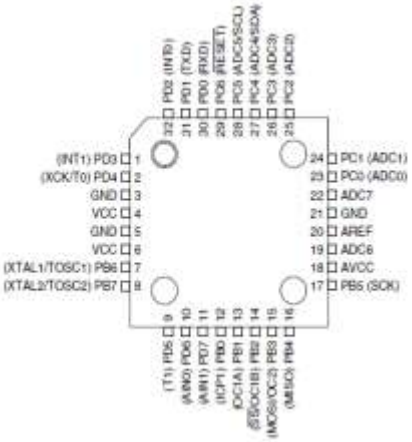
ATmega8(L)

Pin Configurations

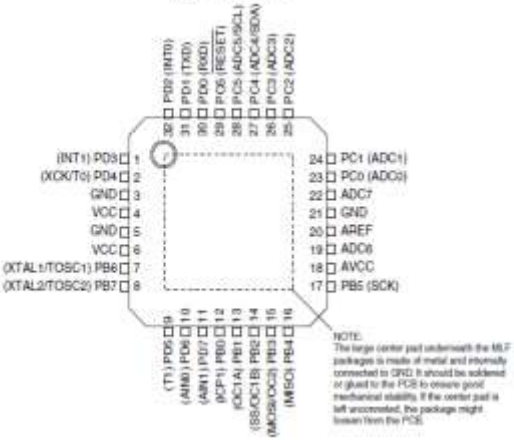
PDIP



TQFP Top View



MLF Top View



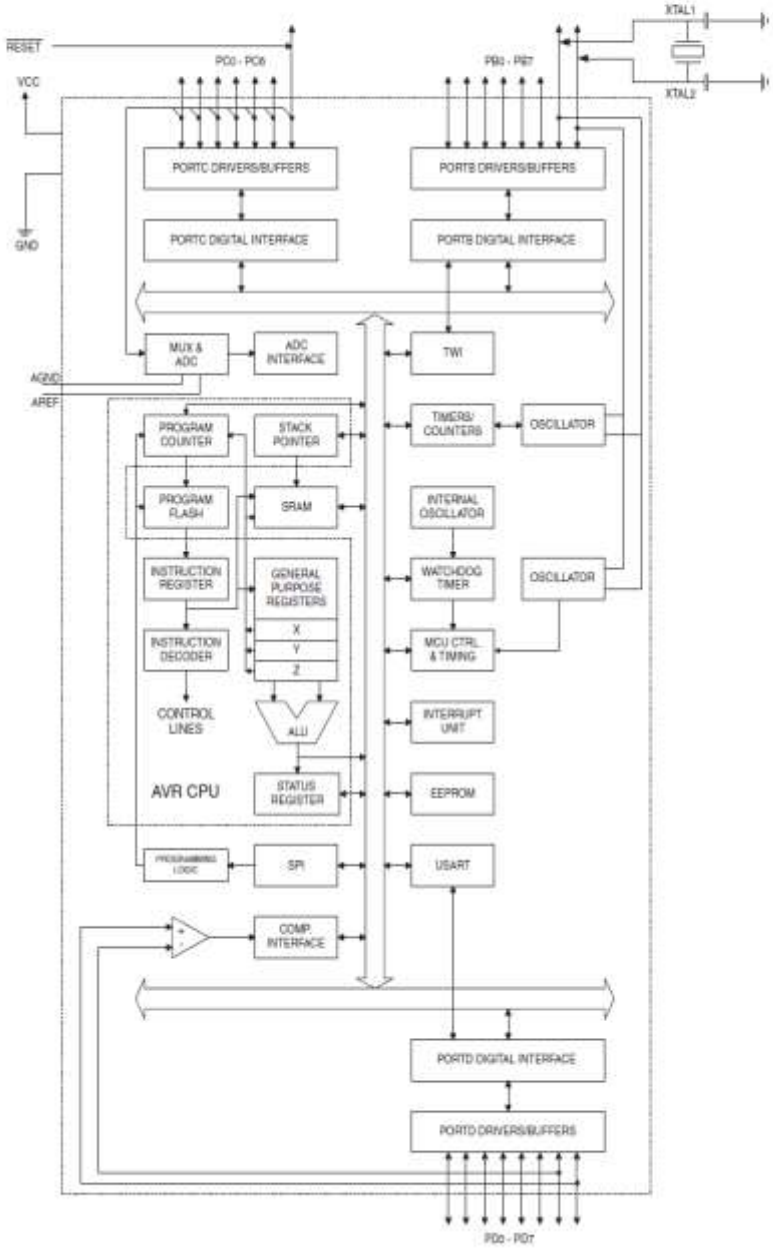
ATmega8(L)

Overview

The Atmel®AVR® ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 1. Block Diagram



ATmega8(L)

The Atmel®AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8 provides the following features: 8 Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes of EEPROM, 1 Kbyte of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, a 6-channel ADC (eight channels in TQFP and QFN/MLF packages) with 10-bit accuracy, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash Program memory can be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash Section will continue to run while the Application Flash Section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega8 is supported with a full suite of program and system development tools, including C compilers, macro assemblers, program simulators, and evaluation kits.

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 16K Bytes of In-System Self-programmable Flash program memory
  - 512 Bytes EEPROM
  - 1K Byte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[1]
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    - 8 Single-ended Channels
    - 7 Differential Channels in TQFP Package Only
    - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega16A
- Speed Grades
  - 0 - 16 MHz for ATmega16A
- Power Consumption @ 1 MHz, 3V, and 25°C for ATmega16A
  - Active: 0.6 mA
  - Idle Mode: 0.2 mA
  - Power-down Mode: < 1µA

ATMEL®

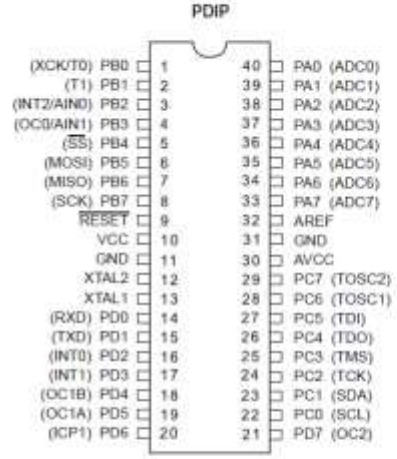
8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

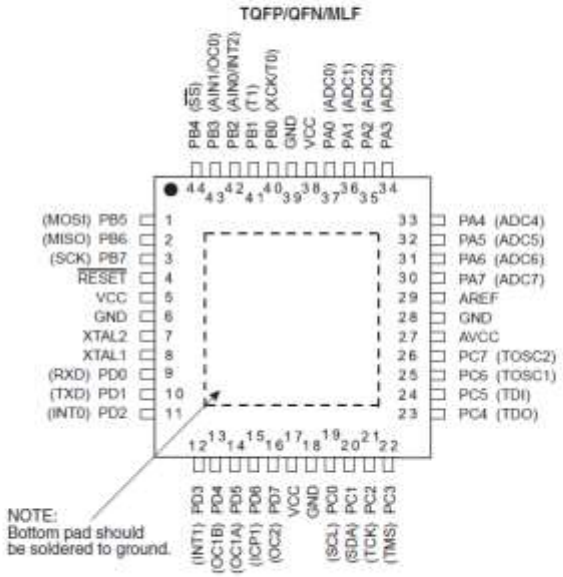
ATmega16A

8154B–AVR–07/09

1. Pin Configurations

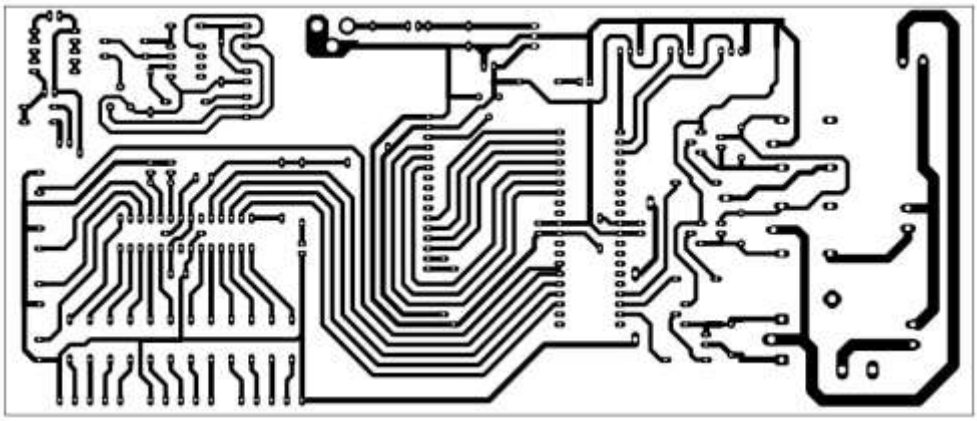
Figure 1-1. Pinout ATmega16A



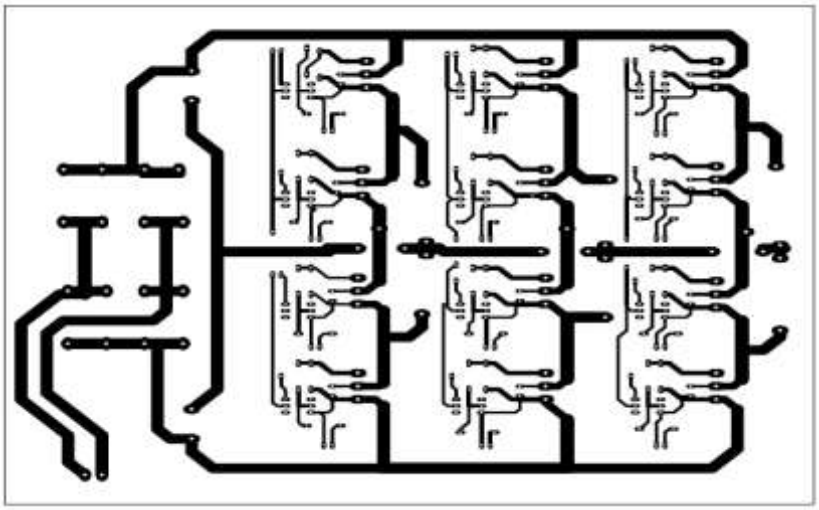


2. Overview

The ATmega16A is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16A achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.



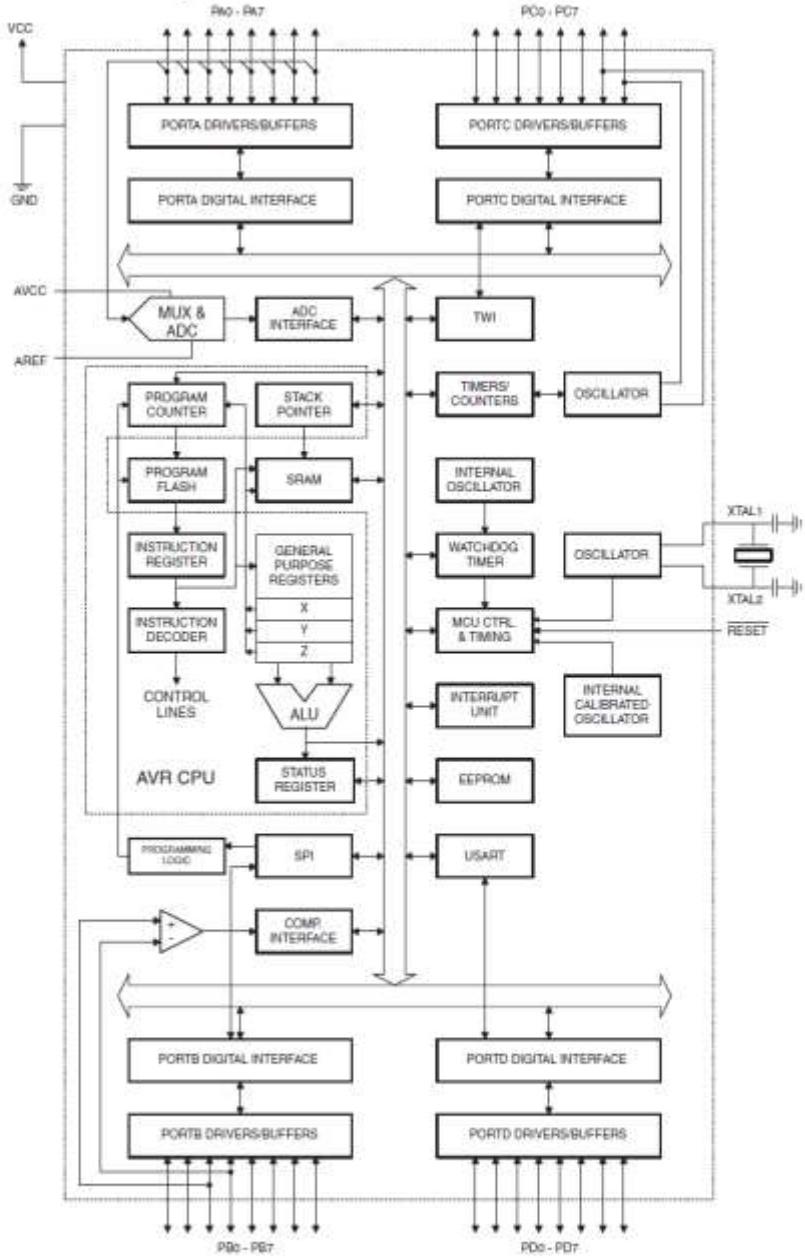
Control and monitor PCB



Three level diode clamped inverter PCB

2.1 Block Diagram

Figure 2-1. Block Diagram



ATmega16A

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega16A provides the following features: 16K bytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1K byte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega16A is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega16A AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.